Progress in and potential of liquid phase crystallized silicon solar cells

Cham Thi Trinh[a], Rutger Schlatmann[b], B. Rech[a], Daniel Amkreutz[a*],

[a)]Institute Silicon Photovoltaics, Helmholtz-Zentrum Berlin für Materialien und Energie GmbH (HZB), Berlin, Germany

[b)]PVcomB, Helmholtz-Zentrum Berlin für Materialien und Energie GmbH (HZB), Berlin, Germany

Corresponding author: daniel.amkreutz@helmholtz-berlin.de, phone: +49 (0) 30 8062-15487

Abstract

Liquid phase crystallization of silicon (LPC-Si) offers great potential for high-quality Si films and a cost effective fabrication technique for thin crystalline silicon solar cells on glass. In this work, we report on the progress on LPC-silicon at HZB in the past years. Beginning with a brief description of the fabrication process, we summarize the work on the different contact systems developed for these absorbers before focusing on the interdigitated back contact architecture on which the highest efficiencies were reported. State-of-the art cells form the basis for a detailed discussion of the status of this technology. We investigate the current loss mechanisms and explore the potential for further improvement. Finally, based on this comprehensive quality assessment, we develop a roadmap to increase the cell efficiencies to wafer-equivalent values.

Introduction

In this work, we review on the progress on crystalline silicon on glass formed using liquid phase crystallization (LPC) method. This technology enables the direct growth of multi-crystalline silicon layers on glass substrates as alternative to standard wafer based photovoltaics. LPC can be a considered as an alternative method to conventional ingot casting and wafering. In the past years, a significant improvement in both maximum open circuit voltage – as parameter for bulk & surface quality – as well as conversion efficiency was demonstrated (figure 1). Recently, we showed a new in-house record of 14.2% on a silicon heterojunction solar cell with interdigitated back contact (IBC) system [Trinh18]. The application of such a design was made possible by careful optimization of the materials used for front-side passivation. That is, the layer stack between glass substrate and absorber (interlayer, IL). The focus on this paper lies on the requirements and comparison of contact systems that can be applied to LPC absorbers on glass. First, we describe briefly the fabrication process of the absorbers, followed by a summary of the morphological and electronic properties. This section provides the requirements on the contact system, followed by a short overview of the different concepts and results achieved in the past. Next, we focus on the design rules for IBC cells and present the influence of the contact geometry on the electronic performance of these devices. Finally, we summarize the current status of liquid phase crystallized silicon on glass and discuss the present limitations. The aim is to provide a roadmap for the further development of LPC-Si in order to achieve efficiencies over 18% on module level.
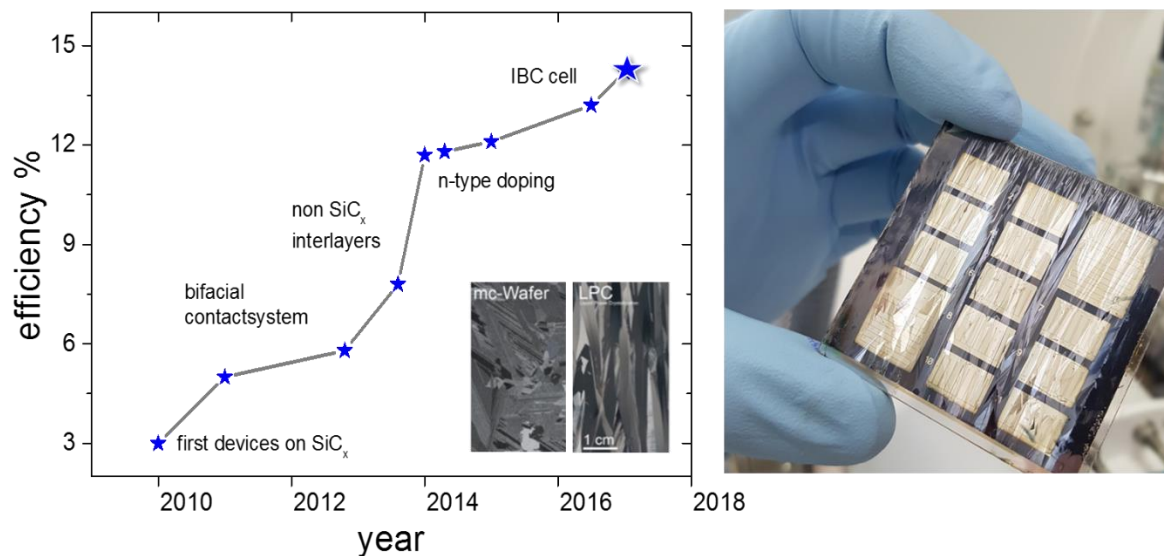
Figure 1: Efficiency progress for liquid phase crystallized silicon solar cells at Helmholtz-Zentrum Berlin (HZB) and future roadmap. Inset: comparison of grain structure of LPC-Si with multi-crystalline wafer (left). IBC cells on liquid phase crystallized silicon on glass (right)

Formation and properties of LPC absorbers

During the past years, different substrates, deposition processes and materials were investigated by us and other groups [Plentz14, Dore13] to increase the electronic and / or optical quality of LPC silicon. In this section we first describe the deposition process and materials used for our current state of the art LPC absorbers. Possible alternatives are described at the end of this section. Beginning with an alkaline glass cleaning step using a aqueous solution of Mucasol® in a commercial glass washing machine (Miele), a interlayer stack is deposited on the Corning Eagle XG 1.1mm thick glass substrates by means of plasma enhanced chemical vapor deposition (PECVD). Best results are achieved using a triple stack of silicon dioxide (SiO_x thickness 220nm), silicon nitride (SiN_x, thickness 65nm) and subsequent plasma oxidization in N_2O ambient to form an approximately 10 nm thin oxynitride layer ($SiON_x$). Whereas the first oxide layer acts as diffusion barrier, the combination of the nitride and oxynitride provides both anti-reflective-properties (AR) and a high level of surface passivation, combining field effect and chemical passivation [Preissler17a]. Next, the silicon precursor layer is deposited by high-rate electron-beam evaporation at surface temperatures of 500°C and a deposition rate of 500 nm/min. At this step no dopants are provided to avoid cross-contamination of the deposition system when switching n- or p-type. Instead, absorber doping is provided by subsequent PECVD deposition of an a-Si:H(n or p) layer followed by a SiO_x capping layer to avoid contamination of the silicon during melt crystallization. The precursor stack is processed without vacuum-break using a Von Ardenne CS400PS integrated PECVD/PVD cluster system. Next, liquid phase crystallization is performed by scanning a line shaped CW-diode laser with constant scanning speed of 3 mm/s over the preheated glass substrates. After crystallization the silicon oxide capping layer is removed using hydrofluoric acid and approximately 300 nm of the top silicon layer is removed using a combination of phosphoric-, nitric-, and hydrofluoric acid (´poly-Si etch´) to remove segregated impurities that might have formed during crystallization. After this treatment, the samples receive a plasma hydrogenation step [Gorka09] to passivate bulk defects such as dangling bonds and further enhance front-side passivation.

Plasma damage is removed by a second poly-Si etch step. For light-trapping, the surface is textured using a simple KOH based treatment to form random pyramids.

Table 1: Comparison of different precursor layer stacks and cells results (SHJ: silicon heterojunction, DJ: diffused junction)

Interlayer stack	IL deposition	contactsystem	Absorber doping	Voc max. [mV]	Eff	Junction type	Ref
ONO	PECVD	IBC	n	651	13.2%	SHJ	[Sonntag17]
ON	PECVD	IBC	n	642	12.5%	SHJ	[Preissler17b]
ON(ON)	PECVD	IBC	n	654	14.2%	SHJ	[Trinh18]
ONO	PVD	FrontERA	n	632	11.8%	SHJ	[Amkreutz14]
NO(ON)	PECVD	PCS	n	649	12.1%	SHJ	[Frijnts15]
ONO	PVD	PCS	p	585	11.7%	DJ	[Dore13]
NO(ON)	PECVD	FrontERA	p	618	11.8%	SHJ	[Frijnts15]

This finalizes the absorber preparation process. Possible alternatives to this process chain used by Helmholtz-Zentrum Berlin or other groups include the usage of Schott Borofloat®33, 3.3mm substrates [Weizman15], PECVD deposition of the interlayer stack and amorphous silicon absorber at low temperatures and subsequent annealing [Gabriel14, Calnan15] or deposition of a single silicon nitride passivation layer [Plentz14]. Table 1 summarizes these alternatives, achieved open circuit voltages and cell efficiencies. Before we concentrate on the contact system design, the absorber morphology is addressed. Figure 2 shows a photoluminescence image of a LPC absorber. The grain structure is clearly visible by grain-boundary recombination. The grains itself show a very low amount of intra-grain defects [Steffens14]. Numerical modelling of test cells and fitting of the measured internal quantum efficiency revealed a diffusion length above the absorber thickness, usually between 10 and 30 micrometers and a very low front surface recombination velocity, below 200 cm/s. However, aside from grain-boundary recombination, regions with a high amount of stacking faults and recombination activity (black circles in figure 2) are present. A detailed investigation by light-beam induced current (LBIC, [Sonntag17b]) and electron-beam induced current mappings (EBIC, [Seifert11]) revealed a significantly lower effective diffusion length below 2 micrometers in these regions. So far no dependency between grain orientation and recombination activity was determined. The grains are mostly random oriented on the substrate surface (5x5 cm or 10x10 cm) with a tendency towards (100) orientation. This tendency can be enhanced by fine-tuning the crystallization parameters [Kühnapfel15]. Measurements of the surface roughness revealed a macroscopic waviness in the mm range of the glass due to stress release during crystallization with an amplitude of approximately 100 micrometers.
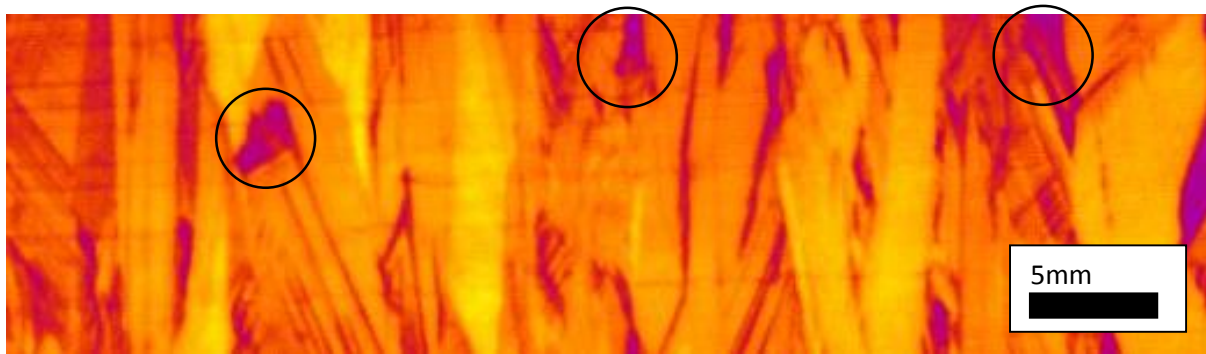
Figure 2: PL image of a liquid phase crystallized absorber to illustrate grain-boundary recombination and regions with high recombination activity due to stacking faults (black circles in the figure).

Contact systems for liquid phase crystallized silicon

Based on the electronic and morphological properties of LPC absorbers presented before, the perquisites for a suitable cell and contact system are discussed. Probably the most obvious requirement is a single-sided approach because after LPC, the silicon-glass interface is not accessible (figure 3). For technological and practical reasons, the illumination – with one exception – will occur from the glass side i.e. superstrate illumination. As the implementation of a front-emitter or BSF or transparent front contact is technologically challenging and was not successfully demonstrated yet, all cell concepts and contact system exhibit a back-junction. This rendered the front-side passivation the most crucial parameter to work on in the past and explains the large amount of work on suitable interlayers [Dore13, Amkreutz14, Plentz14, Gabriel14, Calnan15, Preissler17a, Preissler17b]. Due to the characteristic diffusion length of minority carriers in the absorber layer, the emitter to BSF ratio has to be as large as possible (typically above 90%) to minimize electrical shading. This moves BSF passivation quality and contact resistance into focus for all approaches. Additional technological challenges are present, due to the imperfect surface flatness of the glass substrates after crystallization, which reduces the minimum feature size using photolithography to about 10 micrometers. Alternatively, these challenges can be circumvented using other structuring methods, such as laser ablation or ink-jet printing [Weizman15, Dore13]. Another issue of LPC absorbers is the occasional occurrence of cracks parallel to scanning direction. These cracks are typically between 1mm and 3 mm in length and render point contact systems (like PRECASH [Stangl08]) a suitable choice due to high shunt tolerance. However, it was found that finger-based contact systems can be used, if the fingers are aligned parallel to scanning direction. The first "industrial" contact system used for LPC silicon was initially developed by CSG solar for SPC material [Green04] and later modified by UNSW to fulfill the needs of these multi crystalline absorbers [Dore13]. This point-contact system (PCS) makes use of ink-jet structuring for absorber and emitter contact and the contact pitch is defined by the nozzle spacing of the applied print head. While cell efficiencies up to 11.7% were demonstrated by Dore et al. [Dore13], problems with the stability of the absorber contact were found and successfully avoided by a subsequent laser – firing step [Weizman14] of the absorber contact. Later, a replacement of the ink-jet process by all laser processing was demonstrated by Weizman et al. [Weizman15] and delivered a cell efficiency of 11.5%. As alternative, two finger-based contact systems were developed at HZB during the past years. Initially developed as a bifacial contact system, the so called FrontERA concept was introduced by Haschke et al. [Haschke13]. FrontERA makes use of two vertically aligned grids

for absorber and emitter contacting that are insulated using organic resin. If used in superstrate configuration only, a white paint can be applied as rear reflector. However, at the current state of surface passivation quality the bifacial approach can be omitted in order to reduce process complexity. Especially the absence of an organic resin as insulator, which imposes additional processing and stability issues and the lower complexity gave rise to the development of an interdigitated back-contact system.
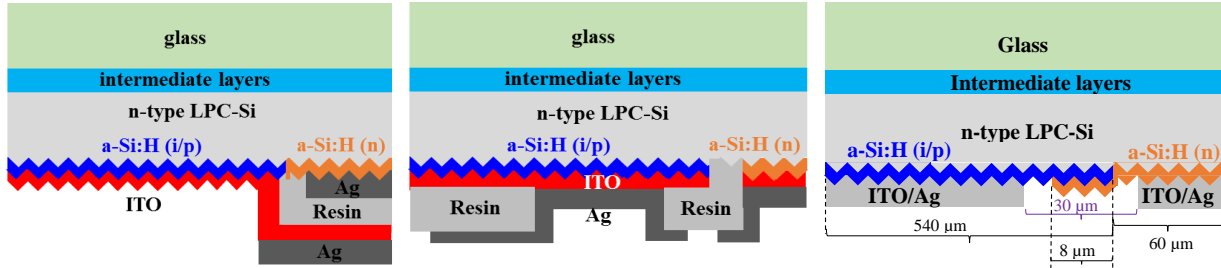

Figure 3: Cross section of the three contact systems applied to liquid phase crystallized silicon on glass: FrontERA bifacial contact system (left), point contact system (PCS, middle), interdigitated back contact system (IBC, right)

Interdigitated back contact cell design for LPC-Si

An IBC-SHJ cell design for LPC-Si was first introduced by Sonntag et al. [Sonntag15]. At that time, besides immature dielectric interlayers (ILs) engineering, IBC-SHJ fabrication process was not fully developed. There are various obstacles for the fabrication process: The first is patterning of the BSF structure, which is almost one order of magnitude narrower than for typical wafer cells due to the lower diffusion length in LPC absorbers. So the BSF width (W_{BSF}) should be as small as possible to prevent minority carrier loss at the BSF. At the same time, it should be large enough to prevent lift-off of the ITO/silver contact of BSF during fabrication process and provide a reliable ohmic contact to the absorber with low series resistance. Therefore, a pitch of 600 μm with W_{BSF} of 60 μm was chosen for the first cells. The second obstacle is back-side surface texturing. Since the absorber is multi crystalline silicon, the surface after texturing includes pyramids, tilted pyramids or flat surfaces depending on initial crystal orientation. Inhomogeneity of the textured surface can lead to inhomogeneous surface passivation and varying contact resistance. Although the initially obtained fill factors (*FF*) for the IBC-SHJ cells shown in [Sonntag15], were lower than 60 %, the high values for the short circuit current density (*J_{sc}*) and open circuit voltage (*V_{oc}*) illustrated the potential of this type of cell on LPC-Si on glass. Later, cells with 13.2% efficiency and FFs of 69% and 75% were achieved for 13 μm-thick LPC-Si absorbers, with both high and low doping (N_D of 1.2×10^{16} and 1.2×10^{17} cm^{-3}), thanks to optimized contact geometry, and development in ILs engineering [Sonntag17]. A larger pitch of 1200 μm and emitter coverage of 0.9 were chosen for contact design since it gives the best compromise between resistive loss and loss due to electrical shading compared to the former cell design. Besides, using metal-ion-free tetramethyl-ammonium hydroxide (TMAH) 2.5% solution for etching a-Si:H (n$^+$) BSF and developing during photolithography process for these cells has advantage of less contamination [Tabata92]. However, analysis of light beam induced current (LBIC) image revealed only poor current

collection under BSF fingers even at areas near the emitter what means that LPC-Si/ BSF interface passivation is still insufficient [Sonntag17, Sonntag17b].

Based on this IBC-SHJ fabrication process, we recently reported cells with 14.2 % efficiency for medium doped LPC-Si absorber (N_D of 8×10^{16} cm^{-3}), using the same contact geometry [Trinh18]. For this cell, J_{sc}, V_{oc} and FF are 29 mA/cm^2, 650 mV and 75 %, respectively. The higher efficiency obtained is due to optimized doping concentration, fine-optimization of the SHJ deposition process, and improvement in ILs engineering. In particular, SiO$_x$/SiN$_x$/SiO$_x$N$_y$ (ON(ON)) ILs, in which SiO$_x$N$_y$ was formed by plasma oxidation, resulted in enhancement of front surface passivation and bulk quality [Preissler17a]. Front surface recombination (SRV$_{front}$) of 100 cm/s and bulk lifetime (τ_{bulk}) of 1.2 μs were estimated for this LPC-Si absorber. The effective diffusion length (L_{eff}) is estimated to 26 μm which is twice the thickness of the absorber. The calculated series resistance of this cell is 1.13 Ωcm^2 which is lower than that of the highly doped 13.2 % efficiency cell (1.32 Ωcm^2), indicating a significantly lower contact resistance.

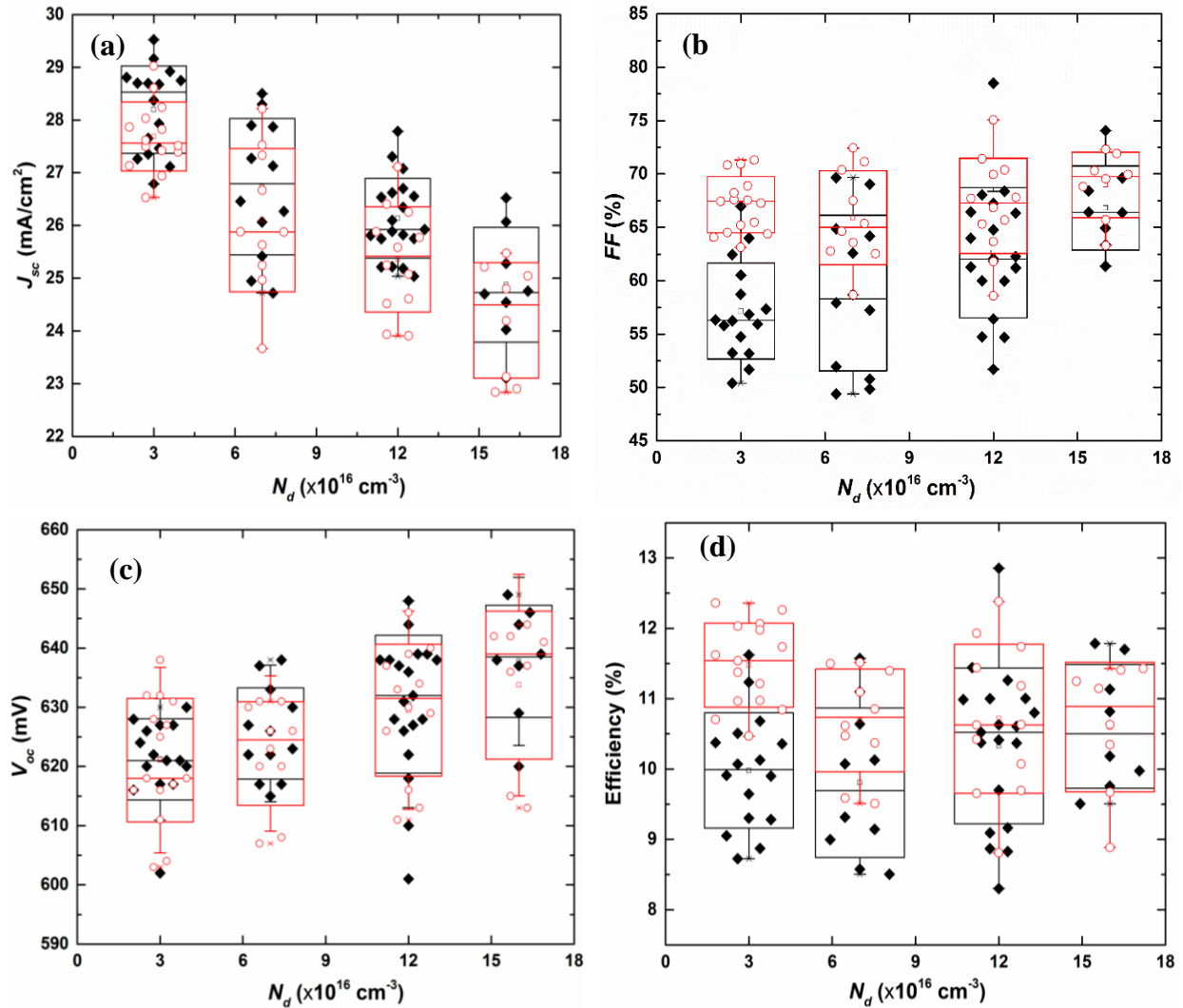**Figure 4:** J_{sc}, FF, V_{oc} and η of IBC-SHJ cells with W_{BSF} of 60 (black diamonds) and 120 μm (open red dots) as functions of dopant density N_D. (measurements without AR foil)

Based on 2D simulations it is concluded that for the IBC cells a BSF width of 60 μm is ideal because it balances between shading loss and resistive loss [Trinh18]. However, this parameter

depends on the doping concentration of the absorber. For the low doped case, where J_{sc} is high due to higher bulk lifetime and correspondingly higher diffusion length, the maximum efficiency is mainly limited by the FF due to contact resistance. Thus, a W_{BSF} of 120 µm is better suited for this dopant concentration to reduce contact resistance. For highly doped absorbers on the other hand, it is possible to obtain high fill factors even for lower values of W_{BSF}, but for this case, efficiency is limited by J_{sc}. For a full understanding, cells with W_{BSF} of 60 and 120 µm were prepared for various doping concentrations. To vary doping concentration, doped source layers (a-Si:H(n+)) were deposited with various phosphine flow rates of 0.2, 0.3, 0.7 and 1 sccm. Absorber preparation and cell fabrication process are the same as in [Sonntag17, Trinh18]. Figure 4 (a)-(d) shows short circuit current density, fill factor, open circuit voltage and efficiency of IBC-SHJ cells as a functions of N_D. One can see that J_{sc} decreases and V_{oc} increases with increasing N_D, as expected. The FF also increases with N_D due to decrease in bulk resistance, especially for W_{BSF} of 60 µm. The average FF for cells with higher BSF width is higher. The difference in average FF of these two cell types becomes smaller when N_D is high, indicating that bulk resistance plays an important role in series resistance when N_D decreases. Consequently, the efficiency, η, of cells with W_{BSF} of 120 µm is higher than that of cells with W_{BSF} of 60 µm for lowly-doped cells. For highly-doped cells, η is in same rage for these two cell types. On the average, lowly-doped cells with W_{BSF} of 120 µm have higher efficiency than other cells, due to the advantage of high J_{sc}, less scattering and reasonable FF. This results suggests that lower doping level is the best choice for further investigation.

In this batch, we are able to achieve a very high fill factor of 78.6 % for a highly-doped cell (N_D of 1.2×10^{17} cm^{-3}) and with W_{BSF} of 60 µm. A conversion efficiency of 14.1 % is obtained if an anti-reflective foil to reduce glass reflectivity and thus enhance light trapping is used. The corresponding J-V curve and parameters of the cell are shown in figure 5 (left) and compared with the previously published 14.2% efficient cell in [Trinh18]. The calculated series resistance amounts to 0.9 Ωcm^2, obtained by comparing dark and illuminated J-V curves according to [Pysch07].
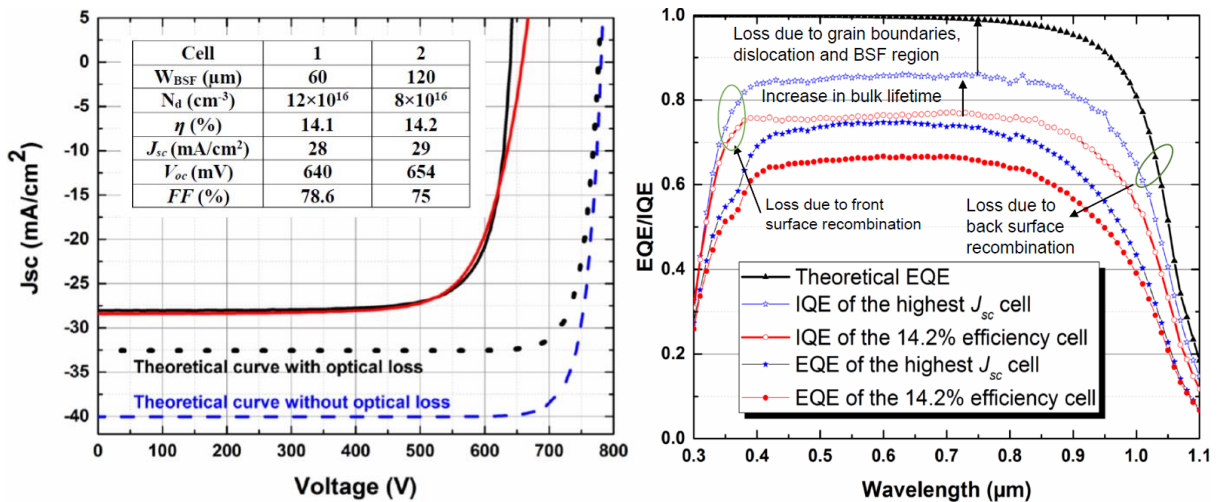

Figure 5: Left: J-V curves of the highest efficiency cells. Cell 1: highly-doped with W_{BSF} of 60 µm (black); cell 2: medium doped W_{BSF} of 120 µm (red) [Trinh18]. Theoretical J-V calculated for N_D of 3×10^{16} cm^{-3} following Ref [Richter13] are also shown. Right: EQE and IQE curves of the highest J_{sc} (29 mA/cm^2) cell with W_{BSF} of 120 µm and N_D of 3×10^{16} cm^{-3}. The curves for the best efficiency cell (14.2%) with N_D of 8×10^{16} cm^{-3} are shown. Theoretical EQE calculated following [Richter13] (right)

This low series resistance is not only attributed to the high doping concentration, but also the fact that this cell exhibits an improved surface texture, compared to the 14.2% efficient cell with a BSF width of 120 μm [Trinh18], resulting in a lower contact resistance due to larger contact area (figure 6). However, an increase in back surface area leads to increase in surface recombination, therefore, this cell has lower V_{oc} and J_{sc} than expected. The high *FF* of 78.6 % demonstrates a great potential for IBC-SHJ cells on glass, indicating optimization of back surface texturing process is a possible way to further increase cell efficiency.
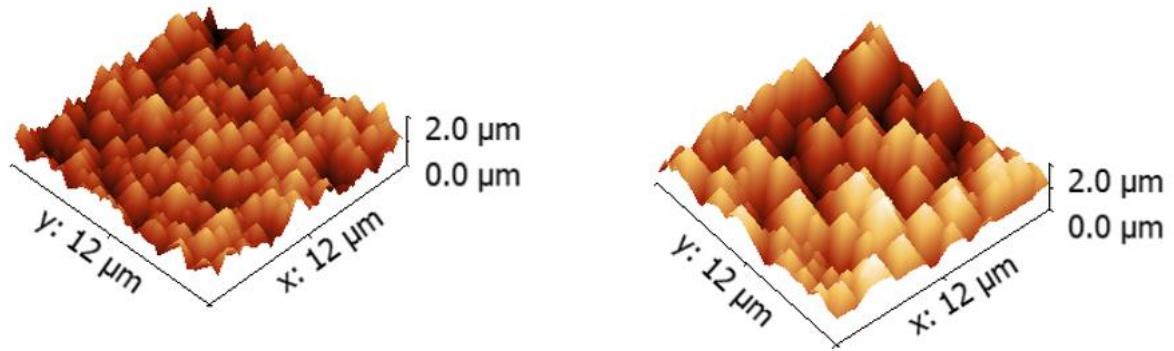

Figure 6: AFM surface micrographs of (111)-surface pyramids of 14.2% efficiency cell with *FF* of 75 % (left), (111)-surface pyramids of 14.1% efficiency cell with *FF* of 78.6 % (right).

Potential of liquid phase crystallized silicon on glass

Based on the experimental results presented in the previous section, we discuss the current loss mechanisms of our cells. Approaches to tackle the present limitations are discussed. This discussion forms the basis for an efficiency roadmap to harvest the full potential of LPC silicon on glass.

Short circuit current density losses

In addition to the experimental *J-V* parameters of our best cells, figure 5 also shows the theoretical *J-V* and EQE curves calculated following reference [Richter13] assuming only intrinsic recombination. Two optical cases were considered: First, ideal optical properties, i.e. no front reflection and assuming Lambertian randomizing light trapping [Richter13] (blue dashed curve in figure 5). Second, with optical losses extracted from GenPro4 [Santbergen17] optical simulations for the full cell stack (glass/ILs/textured LPC-Si/a-Si:H(i/p)/ITO/Ag). For this case, refractive index (*n*) and absorption coefficient (*k*) of SiN_x, SiO_x, SiO_xN_y, a:Si:H and ITO films were determined by using spectroscopic ellipsometry. For other layers, data were taken from literatures [Cushman16, Green08, Johnson72] (black dashed curve in figure 5).

For a cell with thickness of 13 μm and and N_D of 3×10^{16} cm^{-3}, the theoretical efficiency of an ideal electrical and optical cell amounts to 27%, with corresponding J_{sc}, V_{oc} and *FF* values of 40 mA/cm^2, 779 mV and 87 %, respectively. If optical loss is taken into account (i.e. only light that is actually absorbed in Si generates photocurrent), calculated η is 22.3 % with corresponding J_{sc}, V_{oc} and *FF* of 33 mA/cm^2, 775 mV and 87 %, respectively.

According to Sonntag et al. the current loss due to gain boundaries and dislocation rich regions is round 11 % to 14 % [Sonntag17]. This leads to a decrease in J_{sc} to a value of 34.4 - 35.6 mA/cm^2 without and 28.4 - 29.4 mA/cm^2 with optical losses. External- (EQE) and internal quantum efficiency (IQE) of one of the fabricated cells with high J_{sc} (29 mA/cm^2) and a BSF width of 120 µm is plotted in figure 4, right. As shown, a maximum IQE of 0.86 is reached. Compared to the cell with the best efficiency (14.2% [Trinh18]) this illustrates a significantly higher bulk lifetime due to either better intra-grain quality or reduced grain boundary recombination. The experimental J_{sc} of 28-30 mA/cm^2 for cells with lowly-doped absorber (as displayed in figure 4) suggests that for doping level N_D of 3×10^{16} cm^{-3}, L_{eff} should be high enough to collect carriers at BSF region. Therefore, the electronic properties of the cells with this dopant concentration are assessed in the following. In general, most minority carriers will reach the emitter, if

$$L_{eff} \geq \sqrt{\frac{1}{4}W_{BSF}^2 + d_{Si}^2}$$

where d_{Si} is Si thickness (equal to 13 µm). Hence, for efficient minority carrier collection, L_{eff} should be larger than 61 µm and 33 µm, for W_{BSF} of 120 and 60 µm, respectively. To estimate L_{eff} of the samples, TCAD-Sentaurus^{TM} was used to model cell performance, especially J_{sc}, based on the carrier generation profile that was calculated from the Si absorption spectra extracted from GenPro4 (following the method described in [Trinh18]). Next to the generation profile, SRV_{front} values must be considered to evaluate the absorber quality properly. These values were extracted by fitting the obtained J-V and QE results obtained on test cells using numerical simulations e.g. [Sonntag17b]. 2D-simulations of the best performing IBC cells also suggested SRV_{front} of 100-200 cm/s for ONO and ON(ON) ILs [Preissler17b, Sonntag17, Trinh18]. Therefore, SRV_{front} of 100 cm/s was chosen to estimate the lower and upper limits bulk carrier lifetime (τ_{bulk}) for current state of absorber quality. τ_{bulk} was varied until a J_{sc} of 29 mA/cm^2 (the highest experimental value) and 26.5 mA/cm^2 (lowest experimental J_{cs} value) were achieved. As result, a bulk lifetime of 3.7 µs and 1.1 µs are obtained, corresponding to an effective diffusion length of 46 and 26 µm, respectively. As indicated above, the required L_{eff} for full carrier collection at the BSF for cells W_{BSF} of 60 µm was estimated to 33 µm, which could explain that a large number of cells with BSF width of 60 µm were found to have J_{sc} close to the expected values. However, for the cells with W_{BSF} of 120 µm, the required L_{eff} was estimated to be 61 µm, which is larger than the experimentally determined L_{eff}, which may explain that for these samples J_{sc} was found to be lower than 28 mA/cm^2.

Figure 7 shows the expected J_{sc} as function of SRV_{front} and τ_{bulk} of 1.1 and 3.7 µs for IBC cells with dopant concentration $N_D = 3\times10^{16}$ cm^{-3} and BSF width of 120 µm. One can see that J_{sc} starts to decrease strongly when SRV_{front} is larger than 200 cm/s, marking the starting point for domination of front surface recombination on cell performance. For $SRV_{front} < 200$ cm/s, variation in J_{sc} is not significant, indicating cell performance is limited by bulk lifetime. Therefore, improvement in bulk quality is necessary to gain the maximum J_{sc} for cells with W_{BSF} of 120 µm.
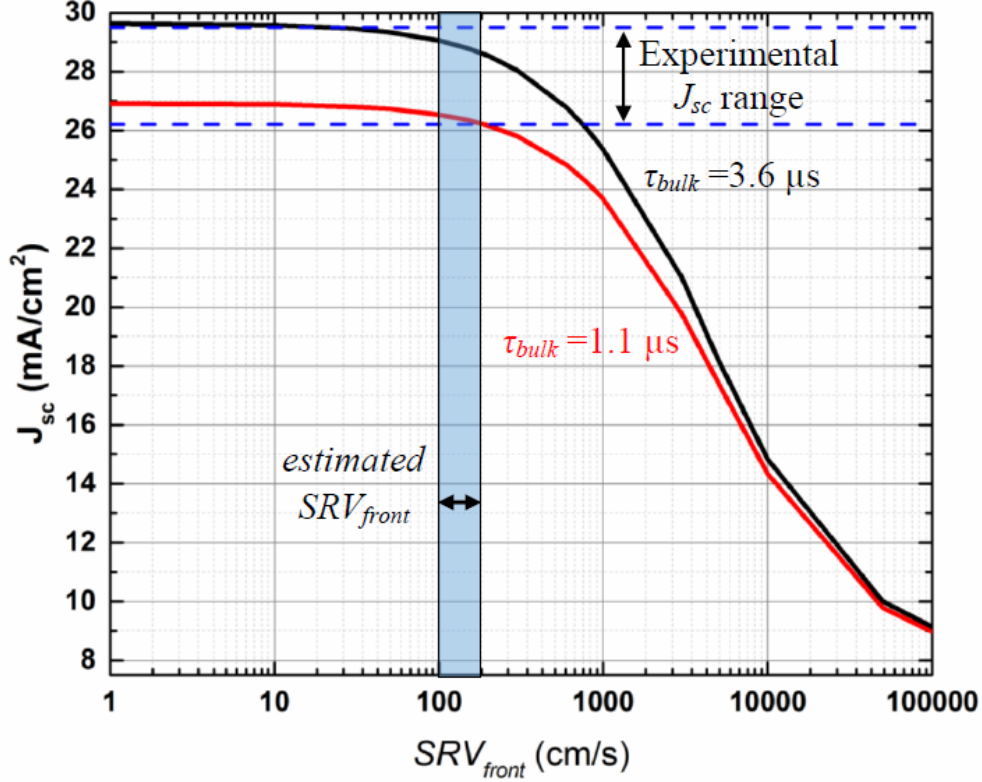
Figure 7: Simulated J_{sc} as functions of SRV_{front} at τ_{bulk} of 1.1 and 3.6 µs for cells with $N_D = 3\times10^{16}$ cm^{-3} and W_{BSF} of 120 µm. Dashed lines indicate minimum and maximum experimental short circuit current density

Short circuit current density and open circuit voltage

Based on the experimental and theoretical results presented before, short circuit current density is limited by absorber bulk quality rather than front side interface recombination. To further increase cell efficiency for the current state-of-the-art absorber quality, one important target is to improve passivation at the absorber contact. As mentioned above, LBIC image indicates that only little current was collected under BSF region, probably due to the missing a-Si:H(i) passivation layer. Although J_{sc} values larger than 28 mA/cm^2 were achieved for some cells with low doping and W_{BSF} of 120 µm, lower J_{sc} values were obtained for almost all cells, implying that photo-generated carriers are not fully collected if they generated in the BSF region. Implementation of a passivation layer to improve back surface passivation could be considered. We have attempted to passivate BSF by an a-Si:H(i). However, S-shape J-V curves were found in the corresponding cells. A possible explanation for S-shaped J-V curves for heterojunction cells has been reported in the literature [Lu11, Kanevce09], focusing on the emitter region, in which thickness and bandgap of a-Si:H(i) play an important role in controlling valence band offset, and tunnel junction for minority carrier transport. However, in our case, S-shaped J-V curves appear only for the case with BSF passivation. One possible reason is incomplete etching of a-Si:H(i) during BSF patterning due to inhomogeneous layer thickness. Since we used KOH-based etching, surface morphology of LPC-Si includes pyramids, tilted pyramids or planar surface. Therefore, the thickness of these ultrathin a-Si:H films are probably not uniform on the sample surface. In our investigation, we used factor of 1.4 to estimate thickness of thin film on textured LPC-Si, i.e, 10 nm thick-a-Si:H (i) film on planar Si wafer was extrapolated to be 7 nm

on textured surface (for a silicon wafer a factor of 1.7 is commonly used [Olibet08]). Therefore, the patterning process of the BSF layer with a passivation layer should be carefully studied. It is found that for deposition of a:Si-H film on textured surface, epitaxial growth and/or formation of cracks in a-Si:H film can occur at the pyramid valleys, which is detrimental to device performance [Lien15, Fresquet09]. The influence of pyramid size distribution on a-Si:H passivation has investigated by Stegemann *et al.* [Stegemann13]. The study suggests that the fraction of small pyramids should be minimized in order to achieve good surface passivation. Therefore, development of texturing process is a promising way to meet this requirement. In addition, rounded pyramids are beneficial for increasing surface passivation, since void formation at the "valleys" or tips during PECVD growth is minimized [Zin17]. Figure 8 shows a textured surface before and after wet chemical etching using aqueous solution consisting of HF, HNO$_3$, and H$_3$PO$_4$.
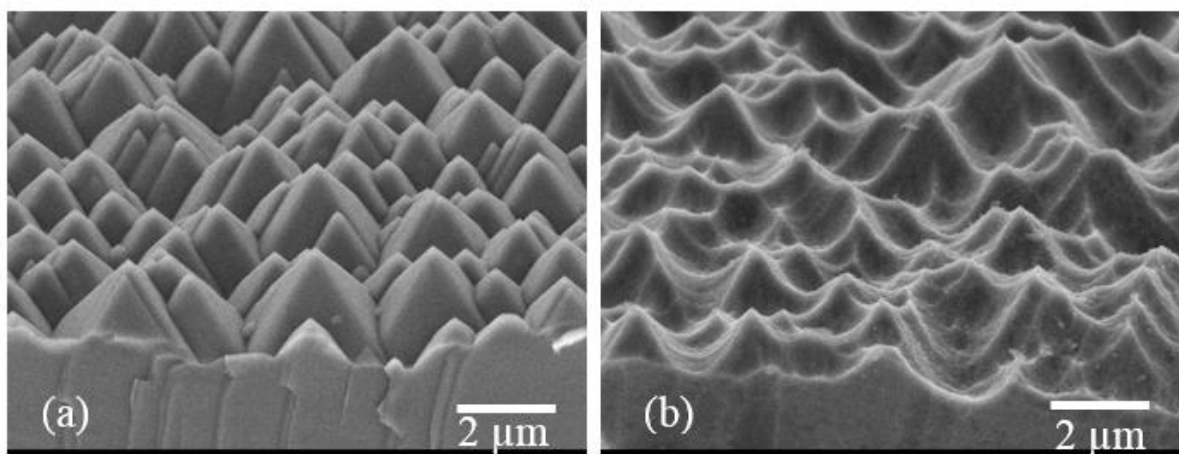

Figure 8: SEM images of a textured LPC-Si on glass (a) before and (b) after wet chemical etching
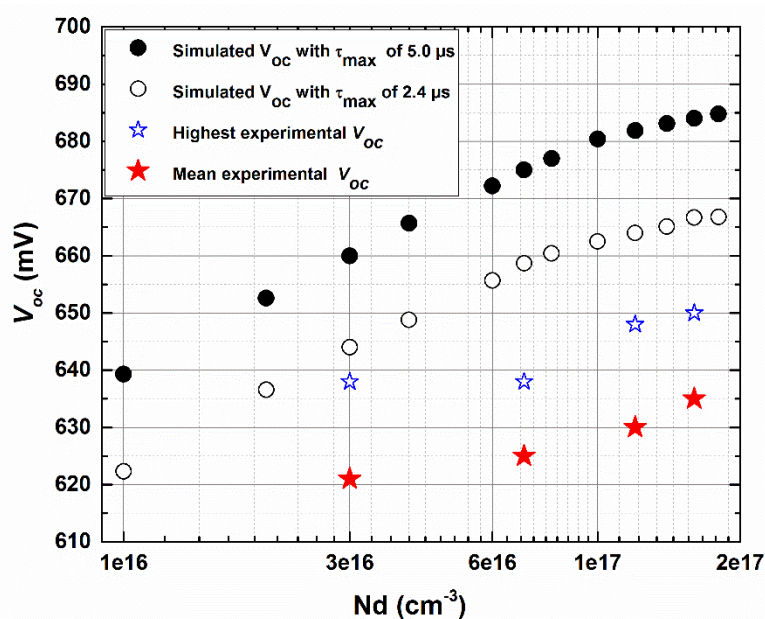

Figure 9: Expected value of the open circuit voltage as a function of absorber dopant concentration with τ_{max} of 5 µs (filled black dots) and 2.4 µs (opened black dots) and comparison with experimental results (blue and red stars)

Concerning the deficiency in open circuit voltage compared to the theoretical maximum given in figure 5, the situation is equally complex as for the current density. According to our simulation in previous literatures [Amkreutz14, Trinh18], a defect layer needed to be introduced to get the best match between simulated V_{oc} and experimental V_{oc}. In order to estimate the expected V_{oc} for the current state of absorber quality, 2D-simulations for IBC-SHJ cell without this defect layer at the SHJ were performed. For this simulation, doping dependent Shockley-Read-Hall lifetime was estimated based on Scharffeter model [Fossum82]:

$$\tau_{bulk} = \tau_{min} + \frac{\tau_{max} - \tau_{min}}{1 + \left(\dfrac{N_D + N_A}{N_{ref}}\right)^{\gamma}}$$

where, $\tau_{min} = 0$ and $\gamma = 1$ were used for Si. N_{ref} of 7.5×10^{16} cm^{-3} was estimated for LPC-Si [Trinh18]. Two τ_{max} values were taken into account. One is 2.4 µs which corresponds to estimated bulk lifetime of 1.2 µs for absorber quality of 14.2% efficiency cell [Trinh18]. Another is 5 µs which results in the upper limit bulk lifetime of 3.6 µs for N_D of 3×10^{16} cm^{-3}, as shown in figure 7. A constant front surface recombination velocity of 100 cm/s was implemented into the simulation. For the back surface, a SRV of 5 cm/s was used. Carrier mobilities of LPC-Si were assumed to be at 80 % of carrier mobilities of mono c-Si. The result of this simulation provided in figure 9 in which the expected voltages for a real IBC cell including recombination loss is depicted. One can see two major issues. A discrepancy of approximately 10mV between the average and the maximum experimental open circuit voltage and another 10mV - 30mV "loss" between the maximum experimental V_{oc} and the expectation from simulation for the different values of τ_{max}. The first finding can be attributed e.g. to a local variation of the surface quality due to grain orientation and therefore tilt angles of the pyramids. However, as we observe an almost constant difference in open circuit voltage between experimental maximum and prediction, the assumption of a negligible recombination at the c-Si (n) / a-Si:H(i/p) interface might not be valid. This brings surface preparation before SHJ deposition into the focus for future improvement. As for BSF passivation this defect layer could have its physical representation in inhomogeneous layer growth of the a-Si:H(i) layer due to surface morphology or insufficient cleaning of the silicon surface before deposition. Another cause for imperfections at the interface could be the incorporation and segregation of carbon and oxygen related impurities [Becker13, Amkreutz17]. However, as for the current density the improvement of the bulk quality promises a significant increase in open circuit voltage towards 660 mV – 670 mV.

Resistance loss and fill factor

Our calculations indicate that more than 90% of series resistance (R_s) is contributed by contact resistance, mainly at the BSF (a-Si:H(n$^+$)/ITO/Ag) contact due to low contact area. Currently, as describe before an increase of the BSW width will cause electrical shading due to limited effective diffusion length. Therefore, a possible way to reduce contact resistance at BSF region is use nano-crystalline (nc)-Si:H(n$^+$) since it has higher conductivity than a-Si:H(n$^+$) [Frijnts17]. However, it is necessary to passivate LPC-Si surface with a-Si:H(i) passivation layer before nc-Si (n$^+$) deposition to prevent formation of carrier recombination center at LPC-Si surface.

Besides, for a-Si:H(p)/ITO/contact, doping concentration and thickness are critical for device performance since they govern carrier transport by band-to-band tunneling through a-Si:H(p)/ITO interface [Kanevce09]. As mentioned above, due to surface morphology, the thickness of the a-Si:H films varies on textured surface posing a challenge to the optimization of the film thickness. In order to overcome this problem a uniform texturing technique for LPC-Si, such as wet chemical etching or ion etching with a mask may be attractive options. Recently, Stang *et. al* reported that for wafer-based Si SHJ cells, the use of Al instead of an ITO/Ag contact resulted in an increase of *FF* from 69.8% to 78.7% with the assistance of an effective annealing step [Stang17]. However, using evaporated Al is not suitable for the LPC-Si cell design since its adhesion is not good enough for the structuring process with small W_{BSF} of 120 µm or lower. Moreover, it is better for LPC-Si to use ITO/Ag contact since light trapping since plasmonic scattering at the back reflector is more effective for thin film absorber [Dijk16, Holman13].

Tackling the optical loss

So far we reported on the loss in J_{sc} due to recombination. Now we discuss the potential to reduce the optical losses. The first step is to optimize the anti-reflective properties of the current interlayer stack. According to a TEM image of the best ILs of ON(ON), the thickness of these films are 55 and 9 nm for SiN_x and SiO_xN_y, respectively. Our optical simulation for a glass/ILs/LPC-Si/a:Si:H (i/p)/ITO/Ag sample with a textured back surface indicates that 75 nm is optimum value for the SiN_x layer. By increasing the SiN_x thickness, a potential J_{sc} gain of 0.6 mA/cm^2 is calculated.

The Genpro4 simulation furthermore reveals 1.94 mA/cm^2 loss due to ITO absorption [Trinh18]. Optimization of ITO thickness and transparence of the film with reasonable conductivity can improve infrared light absorption in absorber. However, the potential J_{sc} gain is less than 1 mA/cm^2. In order to get a higher J_{sc}, close to theoretical value for a 13 micrometer thin absorber (40 mA/cm^2), light trapping/in-coupling schemes including two sided textures are more effective. The impact of an excellent light trapping scheme to obtain a high short circuit current density can be seen for example in [Green09] where a J_{sc} of 29.5 mA/cm^2 was reached for 1-2 µm thick- SPC-Si on glass by a combination of textured glass and back reflector. However, the implementation of front side texturing is critical using LPC absorbers as grain growth can be affected by steep features of a given texture [Preidel15]. Furthermore, inhomogeneous interlayer deposition by non-conformal growth or porosity of the deposited layers on textured glass can results in deterioration of the absorber quality by increased out diffusion of metal impurities in the glass. Nevertheless, LPC on textured glasses was performed successfully on a specially designed texture. This modulated surface texture (MST) developed by TU Delft [Isabella10] uses small as well as large features that wet chemically transferred directly into e.g. Corning glass. The texture is rather smooth, yet provides a significant enhanced light incoupling into the silicon [Köppel17]. In addition, front surface texturing using nano-imprint SiO_x filled with optically contrasting TiO_x, rendering the layer optically rough but morphologically smooth (referred as Smooth Anti-Reflective Three-dimensional/SMART texture) has been successfully applied for LPC-Si on glass without destroying the electric quality of absorber. An increase in J_{sc} of 3.5 mA/cm^2 was observed for full emitter cell (no back reflector and planar back surface) [Eisenhauer17].

Summary and outlook

We presented liquid phase crystallized silicon absorber on glass as a new method to grow wafer equivalent silicon layers with minimal resource utilization. Requirements for contact systems are described and the results achieved on different concepts described in literature are compared. The focus of this work is on the IBC cell concept since the highest efficiencies were realized using this approach. The current status of the cells is presented and the dominant loss mechanisms are summarized. Based on our experimental data and presented numerical simulations, we can conclude that the way to achieve high efficiencies is to reduce the currently used dopant concentration N_D to a value in the lower to medium 10^{16} cm^{-3} range. This would result in an increase in short circuit current density due to higher diffusion length in the bulk to values up to 29 mA/cm² (without AR foil) and 32 mA/cm² (with AR foil). However, so far this dopant concentration not result in higher efficiencies compared to the results obtained on cells doped in the high 10^{16} cm^{-3} to low 10^{17} cm^{-3} range as these cells are limited by a low fill factor, due to high contact resistance at the BSF. Our results show that this could be compensated by a larger width of the absorber contact, but this increased contact width itself limits the current collection due to electrical shading at the present state of absorber quality. Therefore, the most promising approach on the short term is to reduce the contact resistance by optimized texturing or introduction of nc-Si:H at the BSF. On the voltage side, a comparable large discrepancy of approximately 10 mV between maximum and average measured V_{oc} was determined, illustrating the need to improve the homogeneity of the material further. The observed discrepancy between expected and measured values of the open circuit voltage indicate that recombination at the silicon heterojunction interface cannot be neglected. This loss mechanism manifests itself in a reduced open circuit voltage by about 20mV between expected and average Voc. The physical existence of a layer with significant recombination activity at this interface was not proven yet, but spectroscopy of the interface defect state density seems mandatory to further increase the quality of LPC silicon. As discussed with the current state of the front-side passivation, the focus for future improvements has to lie on improvement bulk and rear surface quality. An increase in bulk lifetime by a factor of 2-3 opens the way towards open circuit voltages up to 660 mV – 670 mV and higher. The bulk quality itself can be enhanced by advanced crystallization resulting in preferential orientation and a reduction in recombination-active grain boundaries [Kühnapfel15] or by altering the absorber deposition process as described in [Amkreutz17]. Furthermore, gettering techniques that are regularly used for multicrystalline wafers can be adapted to LPC-Si to reduce the impurity related recombination. However, low resistance contacting of the absorber is mandatory to make use of the current gain. The final step is to implement 3D textures to maximize the short circuit current density, but this will also increase demands on the low-ohmic contact.
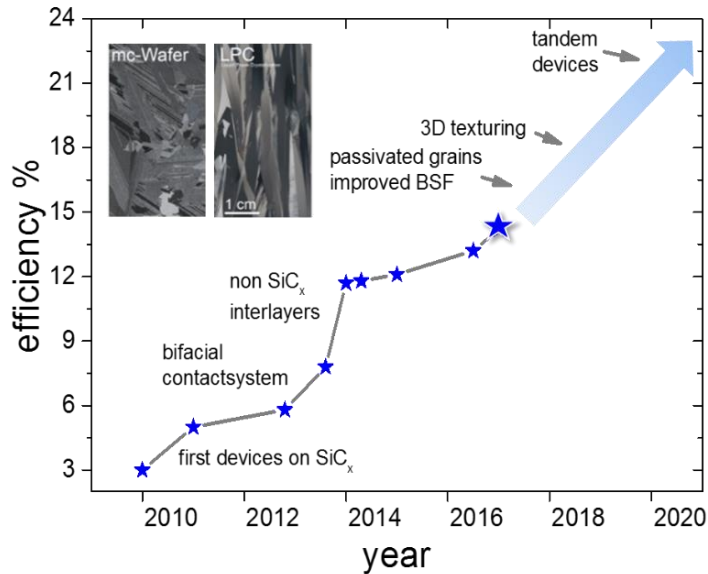
Figure 10: Efficiency progress of liquid phase crystallized silicon on glass and further steps to increase conversion efficiency.

Figure 10 once more shows historic developments, as well a roadmaps with steps to be taken to further increase the efficiency of liquid phase crystallized silicon cells on glass. According to our material investigation we can state that the improvement of BSF passivation and reduce in GB recombination will result in conversion efficiencies up to 16%, further increased to 18% by implementing two sided texturing. Finally, the implementation of LPC-Si as bottom cell in a tandem with a suitable wide-bandgap (e.g. perovskite) top cell is a suitable method to raise efficiencies further.

Literature:

[Amkreutz14] D. Amkreutz et al., "Silicon thin-film solar cells on glass with open-circuit voltages above 620 mV formed by liquid-phase crystallization", IEEE J-PV 4(6), 1496 (2014)

[Amkreutz15] D. Amkreutz et al., "Liquid-Phase Crystallized Silicon Solar Cells on Glass: Increasing the Open-Circuit Voltage by Optimized Interlayers for n- and p-Type Absorbers", IEEE J. PV 5, 1757 (2015)

[Amkreutz17] D. Amkreutz et al. Prog. Photovolt. Res. Appl. DOI: 10.1002/pip.2953 (2017)

[Becker13] C. Becker et al., "Polycrystalline silicon thin-film solar cells: Status and perspectives", Sol. Energy Mater. Sol. Cells 119, 112 (2013)

[Calnan15] S. Calnan et al., "Influence of Chemical Composition and Structure in Silicon Dielectric Materials on Passivation of Thin Crystalline Silicon on Glass", ACS Appl. Mater. Interfaces 7, 19282 (2015)

[Cushman16] C.V. Cushman et al., " Eagle XG® glass: Optical constants from 196 to 1688 nm (0.735-6.33 eV) by spectroscopic ellipsometry", Surf. Sci. Spectra 23, 55 (2016)

[Dijk16] L. Dijk et al., "Plasmonic Scattering Back Reflector for Light Trapping in Flat Nano-Crystalline Silicon Solar Cells", ACS Photonics 3 685−691 (2016)

[Dore13] J. Dore et al., "Progress in laser-crystallized thin-film polycrystalline silicon solar cells: Intermediate layers, light trapping, and metallization", IEEE J. PV 4, 33 (2014)

[Eisenhauer17] D. Eisenhauer et al., "Smooth anti-reflective three-dimensional textures for liquid phase crystallized silicon thin-film solar cells on glass", Sci. Rep. 7, 2658 (2017)

[Frijnts15] T. Frijnts et al., "Analysis of photo-current potentials and losses in thin film crystalline silicon solar cell", Sol. Energy Mater. Sol. Cells 143, 457 (2015)

[Frijnts17] T. Frijnts, "Polycrystalline silicon solar cells on glass – towards an industry compatible process", Ph.D. Thesis (2017)

[Fossum82] J.G. Fossum et al., "A physical model for the dependence of carrier lifetime on doping density in nondegenerate silicon", Solid-State Electron. 25, 741 (1982)

[Fresquet09] G. Fresquet et al., "Modification of textured silicon wafer surface morphology for fabrication of heterojunction solar cell with open circuit voltage over 700 mV", in Proc. 34th IEEE PVSC, 754-758 (2009)

[Gabriel14] O. Gabriel et al., "PECVD intermediate and absorber layers applied in liquid phase crystallized silicon solar cells on glass substrates", IEEE J. PV 4, 1343 (2014)

[Gorka09] B. Gorka et al., "Influence of hydrogen plasma on the defect passivation of polycrystalline Si thin film solar cells", Plasma Processes and Polymers 6, 36 (2009)

[Green04] M.A. Green et al., "Crystalline silicon on glass (CSG) thin-film solar cell modules", Sol. Energy 77, 857 (2004)

[Green08] M.A. Green et al., "Self-consistent optical parameters of intrinsic silicon at 300K including temperature coefficients", Sol. Energy Mater. Sol. Cells 92, 1305 (2008)

[Green09] M. A. Green et al., "Polycrystalline silicon on glass for thin-film solar cells", Appl. Phys A 96, 153 (2009)

[Gref16] O. Gref et al., "Grain boundary light beam induced current: A characterization of bonded silicon wafers and polycrystalline silicon thin films for diffusion length extraction", Phys. Stat. Sol. A 213, 1728 (2016)

[Haschke13] J. Haschke et al., "Polycrystalline silicon heterojunction thin-film solar cells on glass exhibiting 582 mV open-circuit voltage", Sol. Energy Mater. Sol. Cells 115, 7 (2013)

[Haschke16] J. Haschke et al., "Liquid phase crystallized silicon on glass: Technology, material quality and back contacted heterojunction solar cells", Jpn. J. Appl. Phys. 55 04EA04 (2016)

[Holman13] Z.C. Holman et al., "Infrared light management in high-efficiency silicon heterojunction and rear-passivated solar cells", J. Appl. Phys. 113, 013107 (2013)

[Isabella10] O. Isabella, et al., "Modulated surface textures for enhanced light trapping in thin-film silicon solar cells", Appl. Phys. Lett. 97, 101106 (2010)

[Isabella14] O. Isabella et al., "Full-wave optoelectrical modeling of optimized flattened light-scattering substrate for high efficiency thin-film silicon solar cells", Prog. Photovolt. Res. Appl. 22, 671 (2014)

[Johnson72] P. B. Johnson et al., "Optical Constants of the Noble Metals", Physical Review B 6, 4370 (1972)

[Kanevce09] A. Kanevce et al., "The role of amorphous silicon and tunneling in heterojunction with intrinsic thin layer (HIT) solar cells", J. Appl. Phys. 105, 094507 (2009)

[Köppel17] G. Köppel et al., "Periodic and Random Substrate Textures for Liquid-Phase Crystallized Silicon Thin-Film Solar Cells", IEEE J-PV 7(1), 85 (2017)

[Kühnapfel15] S. Kühnapfel et al., "Towards monocrystalline silicon thin films grown on glass by liquid phase crystallization", Sol. Energy Mater. Sol. Cells 140, 86 (2015)

[Lu11] M. Lu et al., "Optimization of interdigitated back contact silicon heterojunction solar cells: tailoring hetero-interface band structures while maintaining surface passivation", Prog. Photovolt: Res. Appl. 19, 326–338 (2011)

[Lien15] S-Y. Lien et al., "Influence of Surface Morphology on the Effective Lifetime and Performance of Silicon Heterojunction Solar Cell", International Journal of Photoenergy, 273615 (2015)

[Olibet08] S. Olibet et al., "Textured Silicon Heterojunction Solar Cells With Over 700 mV Open-Circuit Voltage Studied by Transmission Electron Microscopy", in Proc. 22nd EUPVSEC; Valencia, Spain, 2008; pp 1140– 1144

[Plentz14] J. Plentz et al., "Polycrystalline silicon thin-film solar cells prepared by layered laser crystallization with 540 mV open circuit voltage", Thin. Sol. Films 562, 430 (2014)

[Preidel15] V. Preidel et al., "Balance of optical, structural, and electrical properties of textured liquid phase crystallized Si solar cells", J. Appl. Phys. 117, 225306 (2015)

[Preissler17a] N. Preissler et al., "Interface Engineering for Liquid-Phase Crystallized-Silicon Solar Cells on Glass", Solar RRL 1, 1700015 (2017)

[Preissler17b] N. Preissler et al., "Impact of Dielectric Layers on Liquid-Phase Crystallized Silicon Solar Cells", IEEE J. PV (accepted)

[Preissler18] N. Preissler et al., in preparation (2018)

[Pysch07] D. Pysch et al., "A review and comparison of different methods to determine the series resistance of solar cells", Sol. Energy Mater. Sol. Cells 91, 1698 (2007)

[Richter13] A. Richter et al., "Reassessment of the Limiting Efficiency for Crystalline Silicon Solar Cells", IEEE J. PV 3, 1184 (2013)

[Santbergen17] R. Santbergen et al., "GenPro4 Optical Model for Solar Cell Simulation and Its Application to Multijunction Solar Cells", IEEE J. PV 7, 919 (2017)

[Seifert11] W. Seifert et al., "Analysis of electron-beam crystallized large grained Si films on glasssubstrate by EBIC, EBSD and PL", Solid State Phenomena 178-179, 116 (2011)

[Stang17] J.-C. Stang et al., "Optimized Metallization for Interdigitated Back Contact Silicon Heterojunction Solar Cells", Sol. RRL 1, 1700021 (2017)

[Stangl08] R. Stangl et al.,"Planar rear emitter back contact amorphous/crystalline silicon heterojunction solar cells (RECASH / PRECASH)", in Proc. 33rd IEEE PVSC, 4922756 (2008)

[Steffens14] S. Steffens et al., "Impact of dislocations and dangling bond defects on the electrical performance of crystalline silicon thin films", Appl. Phys. Let. 105, 022108 (2014)

[Stegemann13] B. Stegemann et al., "Passivation of textured silicon wafers: Influence of pyramid size distribution, a-Si:H deposition temperature, and post-treatment", Energy Procedia 38, 881 – 889 (2013)

[Sonntag15] P. Sonntag et al., "Properties of Liquid Phase Crystallized Interdigitated Back-contact Solar Cells on Glass", Energy Procedia 77, 487–492 (2015)

[Sonntag17] P. Sonntag et al., "Silicon solar cells on glass with power conversion efficiency above 13% at thickness below 15 micrometer", Sci. Rep. 7, 873 (2017)

[Sonntag17b] P. Sonntag et al., "Liquid phase crystallized silicon - A holistic absorber quality assessment", Sol. Energy Mater. Sol. Cells in press DOI: 10.1016/j.solmat.2017.08.019 (2017)

[Synopsis] SYNOPSYS. Sentaurus Structure Editor User Guide. F-2011.09, September 2011

[Tabata92] O. Tabata et al., "Anisotropic etching of silicon in TMAH solutions", Sensors and Actuators A: Physical 34, 51 (1992)

[Trinh18] C. Thi-Trinh et al., "Potential of interdigitated back-contact silicon heterojunction solar cells for liquid phase crystallized silicon on glass with efficiency above 14%", Solar Energy Materials and Solar Cells 174, 187-195 (2018)

[Weizman14] M.Weizman et al., "Efficiency and stability enhancement of laser-crystallized polycrystalline silicon thin-film solar cells by laser firing of the absorber contacts", Sol. Energy Mater. Sol. Cells 120, 521 (2014)

[Weizman15] M.Weizman et al., "Rear-side All-by-Laser Point-contact Scheme for liquid-phase-crystallized silicon on glass solar cells", Sol. Energy Mater. Sol. Cells 137, 280 (2015)

[Zin17] N. Zin *et al.*, "Rounded rear pyramidal texture for high efficiency silicon solar cells,", in Proc. 43rd IEEE PVSC, 2548 (2016)