Aluminium metallisation for interdigitated back-contact silicon heterojunction solar cells

Johann-Christoph Stang[1*], Jan Haschke[1,3], Mathias Mews[1], Agnes Merkle[2], Robby Peibst[2], Bernd Rech[1], and Lars Korte[1]

[1] *Helmholtz-Zentrum Berlin, Institute of Silicon Photovoltaics, 12489 Berlin, Germany*

[2] *Institute for Solar Energy Research Hameln, 31860 Emmerthal, Germany*

[3] *École Polytechnique Fédérale de Lausanne (EPFL), Institute of microengineering (IMT), Photovoltaics and Thin Film Electronics Laboratory, CH-2000 Neuchâtel, Switzerland*

*E-mail: johann-christoph.stang@helmholtz-berlin.de

Back-contact silicon heterojunction solar cells with an efficiency of 22% were manufactured, featuring a simple aluminium metallisation directly on the doped amorphous silicon films. Both the open-circuit voltage and the fill factor heavily depend on the parameters of the annealing step after aluminium layer deposition. Using numerical device simulations and in accordance with the literature, we demonstrate that the changes in solar cell parameters with annealing can be explained by the formation of an aluminium silicide layer at temperatures as low as 150°C, improving the contact resistance and thus enhancing the fill factor. Further annealing at higher temperatures initialises the crystallisation of the amorphous silicon layers, yielding even lower contact resistances, but also introduces more defects, diminishing the open-circuit voltage.

1. Introduction

Interdigitated back-contact (IBC) cells based on the silicon heterojunction (SHJ) architecture have proven to deliver outstanding efficiencies.[1-3] No contact grid is required on the cell's front side, which maximises the light absorption and therefore grants very high current densities, while good passivation and selective contacts, inherent to the heterojunction technology, allow for very high open-circuit voltages (V_{OC}).[4] As in conventional back-contact cells, patterning the rear side with a suitable contact geometry poses a major challenge also in IBC-SHJs.[5,6] Taking into account the relatively high contact resistivities of heterojunction solar cells, the inherent marked reduction in contact area further complicates achieving a low series resistance and thus a high fill factor (FF). To guarantee a low series resistance, high-efficiency standard heterojunction cells feature a transparent conductive oxide layer between the amorphous silicon layers and the metallisation on both the front and rear side. Regarding the former, the transparent conductive oxide (TCO) layer must provide a decent lateral conductivity and transparency, and also form an efficient contact with the corresponding amorphous silicon. On the rear side, the TCO layer should enhance mostly the external quantum efficiency (EQE) in the infrared part of the optical spectrum, by suppressing plasmonic absorption effects that occur when the metal is in direct contact with silicon.[7] Owing to the reduction in contact area, having contacts with particularly low contact resistivities becomes increasingly more important when a back-contact architecture is considered; although the contact resistivity between the commonly used indium tin oxide (ITO) layer and an amorphous silicon emitter or back surface field (BSF) layer is sufficiently low when a standard architecture with full-area contacts is used, it is usually too high to ensure a low series resistance and a high FF in back-contact silicon heterojunction cells.[8,9] Recently, alternative materials such as metal oxides have been evaluated as possible TCO materials forming less resistive contacts, especially on p-doped amorphous silicon, owing to an improved band alignment.[10-12] However, it is also possible to fully omit any TCO material by simply using a direct aluminium contact.[13]

In a previous publication, we compared back-contact silicon heterojunction solar cells featuring the popular ITO/Ag contact stack with those using an aluminium contact.[14] Depending on the annealing time and temperature, especially with regard to the Al device, we concluded that the direct Al contact results in a much lower series resistance and therefore a much higher FF at the expense of a significantly reduced V_{OC}. In our particular case, the Al device outperformed the ITO/Ag one slightly (20.7% vs 20.2%). Note that in

other studies, especially those presenting back-contact SHJ solar cells with efficiencies above 25%,[1-3] a TCO is most likely used; however, until now, the exact contact stack in these record devices is unknown.

In this study, we present an update on the previous Al device, which now features an improved front side, leading to higher V_{OC} and short-circuit current density (J_{SC}) values. In addition, we further elaborate the interaction between the aluminium and amorphous silicon layers.

2. Experimental methods

Interdigitated back-contact solar cells were built on ~270-µm-thick float-zone crystalline silicon wafers (n-doped, 1 – 5 Ωcm). The textured front side (alkaline random pyramids) was coated with a double-layer SiN_x stack (10 nm with a refractive index of 2.4, followed by 90 nm with a refractive index of 1.96; these nominal thicknesses refer to a deposition on a planar surface), serving both as a front -side passivation layer as well as an antireflective coating. Intrinsic and doped hydrogenated intrinsic amorphous silicon (a-Si:H) layers (5 and 20 nm thick, respectively) were deposited on the rear side by plasma-enhanced chemical vapour deposition (PECVD; RF of 13.56 MHz for the intrinsic layers, deposited at 170°C; 60 MHz for the doped ones, deposited at 135°C; B_2H_6 and PH_3 were used as precursor gases). A full RCA cleaning was performed before each deposition. First, a stack of intrinsic and p-doped a-Si:H was deposited and structured by photolithography and wet chemistry, followed by the deposition of a stack of intrinsic and n-doped a-Si:H and its patterning. The latter was achieved by etching the i/n-a-Si:H stack with an alkaline solution, which etches intrinsic and n-doped a-Si:H at much higher rates than p-doped a-Si:H. Thus, the already structured p-type a-Si:H layer serves as an etch stop layer and remains practically unharmed during the structuring of the BSF layer. As contact materials, either aluminium or a stack of ITO and silver was chosen. The aluminium was thermally evaporated, while the ITO, as well as the initial 400 nm of silver layer, was sputtered. An additional 1.5 µm silver layer was then thermally evaporated. Both metallisation variants were also structured by photolithography and wet chemistry.

Surface analysis was performed by near-UV photoelectron spectroscopy in the constant final state yield (CFSYS) mode (hv = 3,…,7 eV), using a xenon arc lamp with a double-grating monochromator for excitation and a conventional photoelectron energy analyser (Specs EA-10P) for detection.[15,16]

Synopsys Sentaurus was used to perform numerical simulations[17]. To account for lateral

current flow in a back-contact solar cell, a two-dimensional unit cell was designed on the basis of the dimensions of the real device. A long bulk lifetime (10 ms) and a low front-side surface recombination velocity (5 cm/s) were assumed in order to maximise the effects related to the rear-side contact system of the solar cell. The defect distributions, charge carrier mobilities, and doping levels of the amorphous silicon layers were set to the default values provided by AFORS-HET, a numerical 1D simulation tool for homo- and especially heterostructure solar cells, developed at Helmholtz-Zentrum Berlin.[18)]

3. Results and discussion

Table I shows the AM1.5G-illuminated current density vs voltage (J-V) parameters of cells with aluminium contacts from both batches 1 and 2 as well as those of cells with ITO/Ag contacts from batch 1. In comparison with batch 1, batch 2 features a better front side, which shows improvements in reflectivity and passivation quality (see Fig. 2). Although the cells with the improved front side have a weaker infrared response, they perform slightly better in the much more relevant wavelength range between 600 and 1000 nm. Furthermore, the internal quantum efficiency (IQE) of the batch 2 Al device reaches values close to 100%, while for batch 1, the IQE peaks at around 95%. This clearly indicates an improved front-side passivation and consequently less front-side losses due to recombination.

These improvements mostly affect V_{OC} and J_{SC}. Batch 1 devices featured J_{SC} values of around 40.5 mA/cm^2, while batch 2 devices featured J_{SC} values above 41.5 mA/cm^2. The initial V_{OC} increased by 10 to 15 mV, independent of the metallisation method used.

The FF of the Al devices is strongly affected by annealing. Heating the devices to temperatures of at least 150°C for 10 to 30 min will steadily increase FF. As the overall series resistance is calculated by comparing the light and the dark J-V curves, it decreases accordingly with FF. Note that the hotplate used to anneal batch 1 devices featured a heat reflecting lid, in contrast to that used for batch 2 devices – it is therefore assumed that despite using the same temperature setpoint T_{SET} = 150°C, the hotplate with a lid (HP1) introduces a higher thermal energy to the device than that without a lid (HP2). In the following, mostly results of batch 2 devices will be discussed, meaning that all mentioned temperatures refer to HP2 (if not stated otherwise).

With longer annealing times at sufficiently high temperatures, V_{OC} eventually decreases. If HP1 is used, a total of 15 min at a set temperature of 150°C leads to a marked decrease in V_{OC} for batch 1 devices. A similar effect can be observed with the batch 2 devices, annealed on HP2 at a set temperature of 170°C. At lower temperatures, batch 2 devices could be annealed for an extended period of time without losing any V_{OC}. In contrast, a slight increase of 3 mV was observed.

As already pointed out in our previous report,[14] the simultaneous increase in FF and decrease in V_{OC} result in a trade-off situation and an initially unknown optimal annealing time in order to achieve the maximum efficiency. The best cell in batch 1 reached its maximum efficiency with a rather low final V_{OC} of 649 mV, but with a high FF of 78.7%. Although the best cell in batch 2 also achieved a FF of 78%, its maximum efficiency was already achieved with a FF of 75%, owing to a much higher and more stable V_{OC}. The

implied fill factors (iFFs) determined by minority carrier lifetime measurements are reasonably in both cells:[19] 81.5% for the batch 1 wafer, and 83.2% for the batch 2 wafer. By comparing these values to the corresponding pseudo fill factors (pFF), determined by Suns-V_{OC} measurements, it is possible to distinguish between ohmic and non-ohmic losses[20]. In the case of batch 1, pFF was measured after annealing that strongly impacted the passivation quality and thus V_{OC}, especially in the high injection range. The measured pFF (83.2%) is therefore higher than the aforementioned iFF (81.5%) making it impossible to determine the initial loss contributions by a simple comparison. In the case of batch 2, pFF was determined after reaching the maximum efficiency (for an identical cell on the same wafer as that described in Table I). The resulting value of 82.2% is very close to the obtained iFF, suggesting that only 1%abs of the FF losses are non-ohmic and 7.1 %abs ohmic. The total FF loss (iFF – FF) for batch 1 after the initial annealing step amount to 8.6%abs. Assuming a similar level of non-ohmic losses for batch 2 cells, ohmic losses for batch 1 cells are in line with those of batch 2 cells. Annealing is therefore expected to decrease mainly ohmic losses, as also indicated by total series resistance measurements (see Table I). The current data further suggests that the annealing temperature required to trigger a significant improvement in FF is lower than that required to trigger the rapid deterioration the V_{OC} in both batches 1 and 2. The cause for this behaviour can be determined by understanding the mechanism of interaction of aluminium and amorphous silicon, which will be discussed in the next section.

The interaction of aluminium and amorphous silicon layers after annealing at different temperatures has been studied thoroughly by many researchers. Ishihara *et al.* reported the presence of pits in the amorphous silicon layers produced by the interdiffusion of both aluminium and amorphous silicon at temperatures as low as 170°C.[21] Haque *et al.* studied extensively the aluminium-induced crystallisation of amorphous silicon layers and the subsequent changes in their electrical properties at temperatures ranging from 150 to 300°C.[22,23] Hentzell *et al.* proved the existence of an Al silicide, starting to form at a temperature of approximately 170°C, prior to the silicon crystallisation.[24] Ashtikar *et al.* proposed a detailed model, including a metastable Al silicide layer at the interface at lower temperatures and a gradual crystallisation with increasing temperature.[25]

The effects described in the above-mentioned publications were also used in devices. Schaper *et al.* developed a contact type using the spatial exchange of aluminium and amorphous silicon at higher temperatures to form localised Al contacts through an intrinsic amorphous silicon passivation layer.[26] Bullock *et al.* proposed a passivated Al contact on

heavily diffused homojunction contacts by inserting an intrinsic a-Si layer between the metallisation and the diffused emitter or BSF layer.[27] Current transport was described to occur through a combination of tunnelling and Al spiking.

The aluminium electrodes in our IBC SHJ devices are annealed at comparably low temperatures; thus a full crystallisation or a complete removal of the amorphous layers due to diffusion into the much thicker Al layer is not expected to occur. Annealing the cells at a temperature of 150°C for extended periods of time (up to 35 min) led to a significant improvement in FF and a very slight improvement in V_{OC}. On the basis of the findings of Haque *et al.* and Ashkitar *et al.*, we surmise that a thin Al silicide layer forms at the interface that mostly enhances the contact resistivity without deteriorating the passivating capability of the intrinsic amorphous silicon layer.[22,25] Increasing the annealing temperature up to 170°C should initiate the crystallisation of the a-Si:H material and the strong interdiffusion between the a-Si:H layers and the Al electrode. In this phase, the contact resistivity continues to decrease, as indicated by an ever increasing FF; however, at the same time, the Al electrode introduces defects in the band gap, degrading the passivation of the crystalline silicon surface.[28] Although the new Al defects might even enhance the p-type doping in the emitter region, they will lower the n-type doping in the BSF regions, reducing the field effect passivation at this interface; prolonged annealing can even lead to the counterdoping of n-type amorphous silicon.[23] All these effects eventually result in a substantial reduction in V_{OC}. Further increase in annealing temperature then leads to a strong diffusion of the amorphous silicon material into the Al layer, leaving behind either voids or aluminium regions.

To examine such a thin a-Si:H film on crystalline silicon (c-Si) after Al deposition and annealing, Al/a-Si:H(p)/c-Si(n) test structures were fabricated and analysed by near-UV photoelectron spectroscopy in the constant final state mode (CFS; Fig. 3). Prior to the measurements, one sample (red curve in Fig. 3) was annealed at 150°C (HP1) for 20 min, roughly the same time and temperature that lead to a strong V_{OC} loss in a real solar cell device. Subsequently, the Al film was etched back to expose the a-Si:H layer. A second sample (blue curve) underwent the same process steps, except annealing. It thus represents an a-Si:H bulk film, modified by the chemical treatment used to etch back the Al layer. In Fig. 3, an additional CFS data set is shown; this data set was obtained from an n-type c-Si wafer after RCA cleaning and silicon oxide removal (1 min etching in 1% HF in H_2O). The measurement on the annealed and etched sample can be fitted as the sum of the shifted and scaled latter two spectra, i.e.,

$$Counts(E) = C_{cSi}\, Counts_{aSi}(E-\Delta E_{aSi}) + C_{cSi}\, Counts_{cSi}(E-\Delta E_{cSi}),$$

where $Counts_i(E)$ are the experimental energy-resolved photoelectron counts of the reference spectra, C_{cSi} and C_{aSi} are the fit parameters, i.e., the scaling constants of the two spectra, and ΔE_{cSi} and ΔE_{aSi} are the shifts of those spectra along the energy axis, respectively. In previous publications, we have used the same approach for fitting samples consisting of a c-Si bulk with thin, homogeneous aSi:H overlayers. We calculate the a-Si:H/c-Si valence band offset from $\Delta E_V = \Delta E_{aSi} + \Delta E_{cSi} - (E_F-E_V)_{aSi} - (E_F-E_V)_{cSi}$ to 0.45 eV, which is in accordance with previous findings for the aSi:H/c-Si heterointerface.[29] Taking into account the scanning electron microscope (SEM) images (Fig. 4), we surmise that the measured spectrum results from an a-Si:H film with a thickness above the information depth, i.e., > 1-2nm, with small c-Si regions that are not or are barely (1 to 2 nm) covered with a-Si:H. Unfortunately, the relative contributions of the two bulk reference spectra, expressed by the fitting parameters C_{cSi} and C_{aSi}, cannot be used to quantify the percentage of exposed c-Si surface area, since the samples were measured on different days and the measured data could not be corrected for the resulting different illumination conditions, yielding an additional scaling parameter of the count rates.

Note that the spectrum of the annealed and etched sample shows a significant signal well above the Fermi level, in the binding energy region of approximately +0.2 eV. This emission probably stems from the occupied gap states of the c-Si substrate. Since the a-Si:H/c-Si sample is in contact with the a-Si:H(p) surface, a signal above E_F (E_{bind}=0) must be related either to surface charging or to band bending and/or a different surface dipole between the sample contact area and the origin of the photoelectron emission. Surface charging is unlikely, since the surface consists of a sufficiently conductive layer. Thus, a significant band bending and/or surface dipole difference must exist between the contact area, i.e., the aSi:H(p)/vacuum interface, and the exposed c-Si regions. From the onset of the CFS signal, this energy difference is estimated to be ~500-600 mV, i.e., the order of magnitude of the built-in potential at the aSi:H(p)/c-Si(n) interface.

Thus, the main physical phenomena we expect affect the performance of our IBC SHJ solar cells with Al electrodes are the formation of an Al silicide layer, partial crystallisation, and the formation of Al defects in the a-Si:H material. According to the results of CFSYS analysis, prolonged annealing at temperatures below 200°C already severely damages the

integrity of the a-Si:H layers. From the pits seen on the SEM image of the annealed surface (Fig. 4), we approximate the area being heavily affected by the Al interaction to a maximum of 20%. On the basis of this approximation, we conduct a numerical simulation of our IBC-SHJ device by introducing a modified region into the a-Si:H contact layers with increased charge carrier mobility and defect density accounting for both the partial crystallisation and the introduction of Al defects (see Fig. 5). The minority charge carrier mobility was increased by a factor of 10 (from 5 to 50 $cm^2V^{-1}s^{-1}$), which is in accordance with the measurement results from Nast *et al.* for polysilicon layers on glass, created from amorphous silicon by aluminium-induced crystallisation (glass/Al/a-Si to glass/poly-Si/Al).[30] The parameters for Al defects in silicon layers were determined by Rosenits *et al.*; the energetic position of the defect was then altered to account for the larger bandgap of amorphous silicon.[28] Although our simulation setup already produces reasonable results when compared with an experimental setup, we do not aim to fully reproduce our measurements, but to confirm experimental trends qualitatively. Indeed, despite having made rather vague approximations to incorporate the changes induced by Al annealing, the trends for FF and V_{OC} observed in the measurements are also present in the simulation results: Without any modification, the simulated cell achieves a V_{OC} of 733 mV and a FF of 69.8%. Although V_{OC} is significantly higher than that in real cells, most likely owing to the very good front side passivation, FF is very close to what we usually measure with a non-annealed device. As shown in Fig. 6(a), increasing the charge carrier mobility does lead to a significant increase in FF, also depending on the modified ratio of the contact area. The abscissa of Fig. 6(a) shows only the values for the minority carrier mobility; however, the majority carrier mobility is increased by the same factor, from a default of 20 $cm^2V^{-1}s^{-1}$ up to 200 $cm^2V^{-1}s^{-1}$. In addition, the increase in FF was performed without adding any additional Al defects, as the measurement results suggest that the increase in FF occurs prior to the deterioration of V_{OC}. The eventual simulated FF increase (up to 77%) is in good agreement with the measurement results obtained after heavy annealing. The effect of an additional Al defect density is shown in Fig. 6(b). Increasing the Al defect density up to values within the doping density range (charge carrier mobility kept at the evaluated maximum values) leads to a strong decrease in V_{OC}, again depending on the modified actual area ratio. The losses of 50 to 60 mV are again in good agreement with the measurement results of annealed devices.

4. Conclusions

We have shown that a direct aluminium metallisation can be a viable option for high-efficiency back-contact silicon heterojunction cells. Careful annealing of the aluminium layers is crucial to enhancing the contact resistivity and maximising the fill factor without deteriorating the open-circuit voltage. The interaction of aluminium and amorphous silicon must be limited to the formation of an intermediate Al silicide layer. The extended crystallisation or interdiffusion of aluminium and silicon will, despite further increase in FF, damage the integrity of the amorphous silicon layers and lead to a significant decrease in open-circuit voltage.

Acknowledgments

This work was supported by the European Union's Horizon 2020 Programme for research, technological development and demonstration under Grant Agreement No. 727523 (project NextBase). Furthermore, the authors thank E. Conrad, M. Wittig, K. Jacob, C. Klimm, M. Hartig, H. Kohlenberg, and T. Friedrich for their support in fabricating the solar cells.

References

1) K. Yoshikawa, H. Kawasaki,W. Yoshida, T. Irie, K. Konishi, K. Nakano, T. Uto, D. Adachi, M. Kanematsu, H. Uzu, and Kenji Yamamoto, Nat. Energy, **2**, 17032 (2017).
2) J. Nakamura, N. Asano, T. Hieda, C. Okamoto, H. Katayama, and K. Nakamura, IEEE J. Photovoltaics, **4**, 1491 (2014).
3) K. Masuko, M. Shigematsu, T. Hashiguchi, D. Fujishima, M. Kai, N. Yoshimura, T. Yamaguchi, Y. Ichihashi, T. Mishima, N. Matsubara, T. Yamanishi, T. Takahama, M. Taguchi, E. Maruyama, and S. Okamoto, IEEE J. Photovoltaics, **4**, 1433 (2014).
4) M. Taguchi. A. Yano, S. Tohoda, K. Matsuyama, Y. Nakamura, T. Nishiwaki, K. Fujita, and E. Maruyama, IEEE J. Photovoltaics, **4**, 96 (2014).
5) T. Desrues, S. de Vecchi, G. d'Alonzo, D. Muñoz, and P.-J. Ribeyron, Proc. 40th IEEE Photovoltaic Specialists Conf., 2014. p. 857.
6) A. Tomasi, B. Paviet-Salomon, D. Lachenal, S. Martin de Nicolas, A. Descoeudres, J. Geissbühler, S. DeWolf, and Christophe Ballif, IEEE J. Photovoltaics, **4**, 1046 (2014).
7) Z. Holman, M. Filipic, A. Descoeudres, S. DeWolf, F. Smole, M. Topic, and C. Ballif, J. Appl. Phys., **113**, 13107 (2013).
8) M. Bivour, C. Reichel, M. Hermle, and S. Glunz, Sol. Energy Mater. Sol. Cells, **106**, 11 (2012).
9) S. Lee, H. Choi, H. Li, K. Ji, S. Namb, J. Choi, S. Ahna, H. Lee, and B Parket, Sol. Energy Mater. Sol. Cells, **120**, 412 (2014).
10) C. Battaglia, X. Yin, M. Zheng, I. Sharp, T. Chen, S. McDonnell, A. Azcatl, C. Carraro, B. Ma, R. Maboudian, R. Wallace, and A. Javeyet, Nano Lett., **14**, 967 (2014).
11) M. Bivour, J. Temmler, H. Steinkemper, and M. Hermle, Sol. Energy Mater. Sol. Cells, **142**, 34 (2015).
12) J. Geissbühler, J. Werner, S. Martin de Nicolas, L. Barraud, A. Hessler-Wyser, M. Despeisse, S. Nicolay, A. Tomasi, B. Niesen, S. De Wolf, and Christophe Ballif, Appl. Phys. Lett., **107**, 081601 (2015).
13) N. Mingirulli, J. Haschke, R. Gogolin, R. Ferré, T. Schulze, J. Düsterhöft, N.-P. Harder, L. Korte, R. Brendel, and B. Rech, Phys. Status Solidi, Rapid Res. Lett., **5**, 159 (2011).
14) J.-C. Stang, T. Franssen, J. Haschke, M. Mews, A. Merkle, R. Peibst, B. Rech, and L. Korte, Sol. Rapid Res. Lett., **1**, 1700021 (2017).
15) M. Sebastiani, L. Di Gaspare, G. Capellini, C. Bittencourt, and F. Evangelisti, Phys. Rev. Lett. **75**, 3352 (1995).
16) L. Korte, and M. Schmidt, J. Non-Cryst. Solids, **354**, 2138 (2008).

17) Synopsys, Version J-2014.09, (2014) [www.synopsys.com].
18) R. Varache, C. Leendertz, M. Gueunier-Farret, J. Haschke, D. Muñoz, and L. Korte, Sol. Energy Mater. Sol. Cells, **141**, 14 (2015).
19) M. Leilaeioun, and Z. Holman, J. Appl. Phys., **120**, 123111 (2016).
20) J. Haschke, N. Mingirulli, R. Gogolin, R. Ferré, T. Schulze, J. Düsterhöft, N.-P. Harder, and L. Korte., IEEE J. Photovoltaics, **1**, 130 (2011).
21) S. Ishihara, T. Hirao, K. Mori, M. Kitagawa, M. Ohno, and S. Kohiki, J. Appl. Phys., **53**, 3909 (1982).
22) M. Haque, H. Naseem, and W. Brown, J. Appl. Phys., **75**, 3928 (1994).
23) M. Haque, H. Naseem, and W. Brown, J. Appl. Phys., **79**, 7529 (1996).
24) H. Hentzell, A. Robertsson, L. Hultman, G. Shaofang, S. Hörnström, and P. Psaras, Appl. Phys. Lett., **50**, 933 (1987).
25) M. Ashtikar, and G. Sharma, J. Appl. Phys., **78**, 913 (1995).
26) M. Schaper, J. Schmidt, H. Plagwitz, and R. Brendel, Prog. Photovoltaics, **13**, 381 (2005).
27) J. Bullock, D. Yan, Y. Wan, A. Cuevas, B. Demaurex, A. Hessler-Wyser and S. DeWolf, J. Appl. Phys., **115**, 163703 (2014).
28) P. Rosenits, T. Roth, S. Glunz, and S. Beljakowa, Appl. Phys. Lett., **91**, 122109 (2007).
29) L. Korte, and M. Schmidt, J. Appl. Phys., **109**, 63714 (2011).
30) O. Nast, S. Brehme, D. Neuhaus, and S. Wenham, IEEE Trans. Electron Devices, **46**, 2062 (1999).

Figure Captions

Fig. 1. (Colour online) J-V curves of the three best cells for each metallisation concept/front side. Inset: depiction of the solar cell structure.

Fig. 2. (Colour online) EQE, IQE, and reflection data for Al and ITO/Ag devices from batch 1 (b1) and an Al device from batch 2 (b2, improved front side).

Fig. 3. (Colour online) CFSYS spectra, where the red curve (dashed-dotted) represents the Al-interacted a-Si:H sample, the blue curve (dashed) the non-annealed, non-interacted a-Si:H sample, and the black curve (solid) a pure c-Si sample; the orange curve (dotted) shows the fit of the blue and black curves, being in good agreement with the red curve, thus indicating that the red curve shows a measurement of a partly disintegrated a-Si:H layer on a c-Si surface.

Fig. 4. SEM image of the amorphous silicon surface after the removal of annealed aluminium. The darker areas are pits in the amorphous silicon layer and the white flakes are believed to be residues of the Al silicide layer.

Fig. 5. (Colour Online) Simulated unit cell. Ruled areas represent the aluminium interacted, modified regions with increased mobility and Al defect density; “pit coverage” refers to the portion of the total contact width that has been modified.

Fig. 6. (Colour online) Trends extracted from simulation: (a) shows the effect of an increased charge carrier mobility (both polarities equally increased; the abscissa shows only the values for the minority carriers) on the FF of the device for different affected area ratios (correlating with the pits seen in Fig. 4); (b) shows the effect of an additional Al defect density on the V_{OC} of the device, again for different affected area ratios.

Table I. J-V parameters (solar cells under illumination, b1 = batch 1, b2 = batch 2).

Metallisation concept	ITO/Ag	Al b1 (5 Min 150°C*)	Al b1 (+10 Min 150°C*)	Al b2 (5 Min 150°C)	Al b2 (+30 Min 150 °C +10 Min 160°C)	Al b2 (+10 Min 170°C)
J_{SC} (mA/cm^2)	40.5	40.5	40.5	41.6	41.9	41.6
V_{OC} (mV)	687	684	649	696	699	660
FF (%)	69.1	72.9	78.7	73.8	75.1	78.2
Pseudo-FF (%)	80.1	/	83.4	/	82.2**	/
Efficiency (%)	19.2	20.2	20.7	21.4	22.0	21.5
$R_{SER, Total}$ (Ω*cm^2)	2.08	1.48	0.49	1.41	1.17	0.71

* different hotplates were used for batches 1 and 2
** identical cell on the same wafer

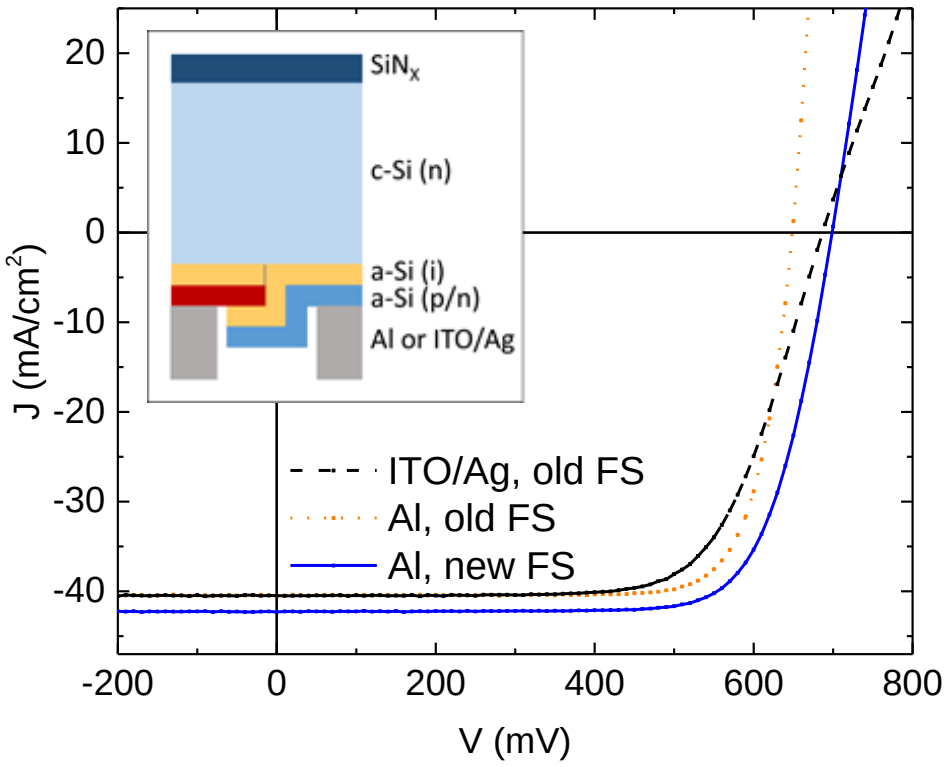

Fig.1. (Colour Online)

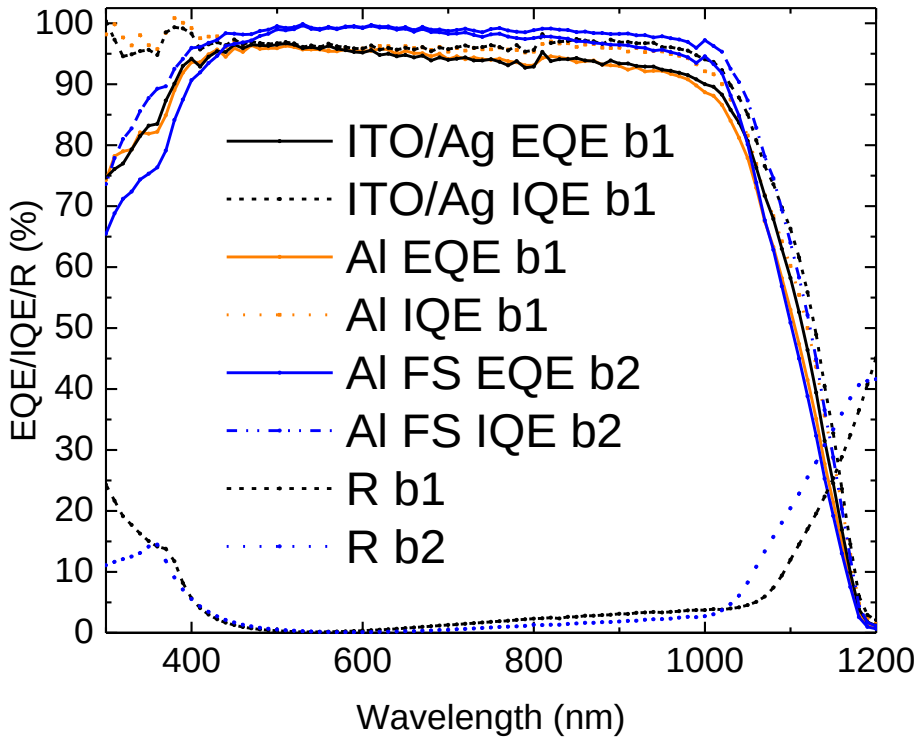

Fig. 2. (Colour online)

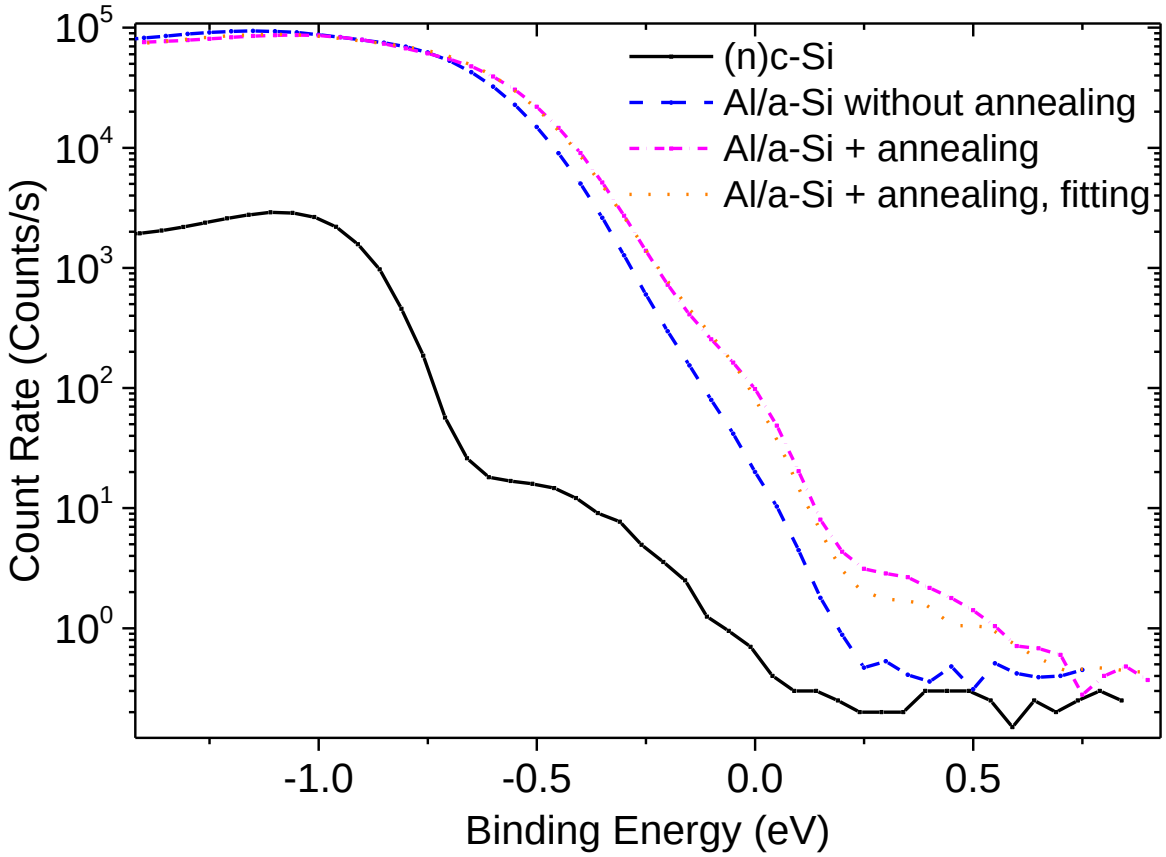

Fig. 3. (Colour online)

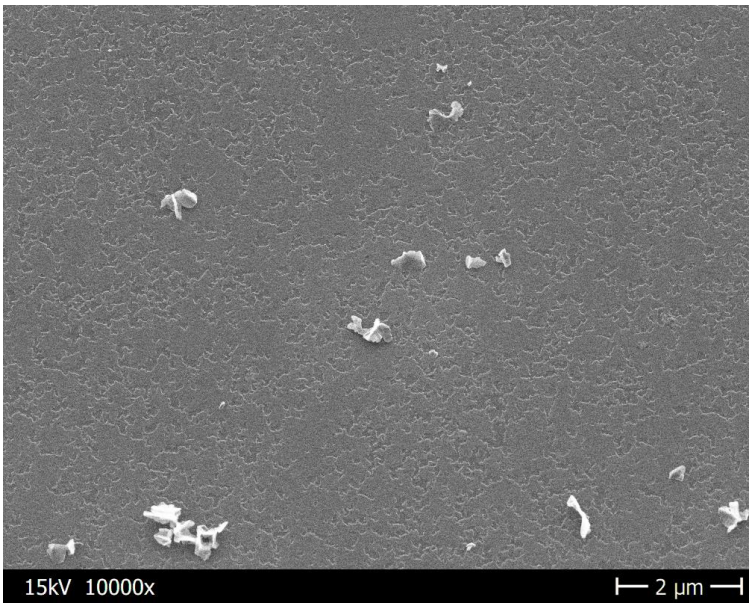

Fig. 4.

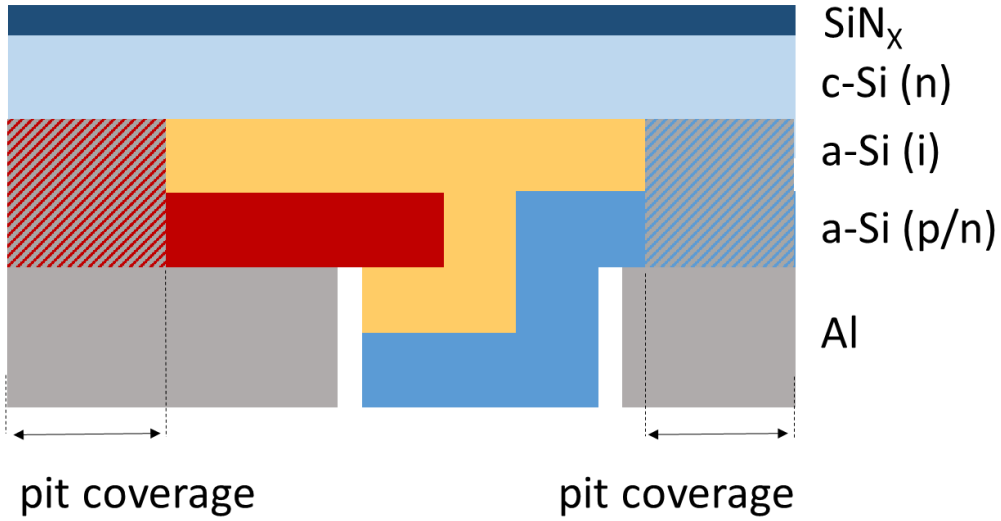

Fig. 5 (Colour online)

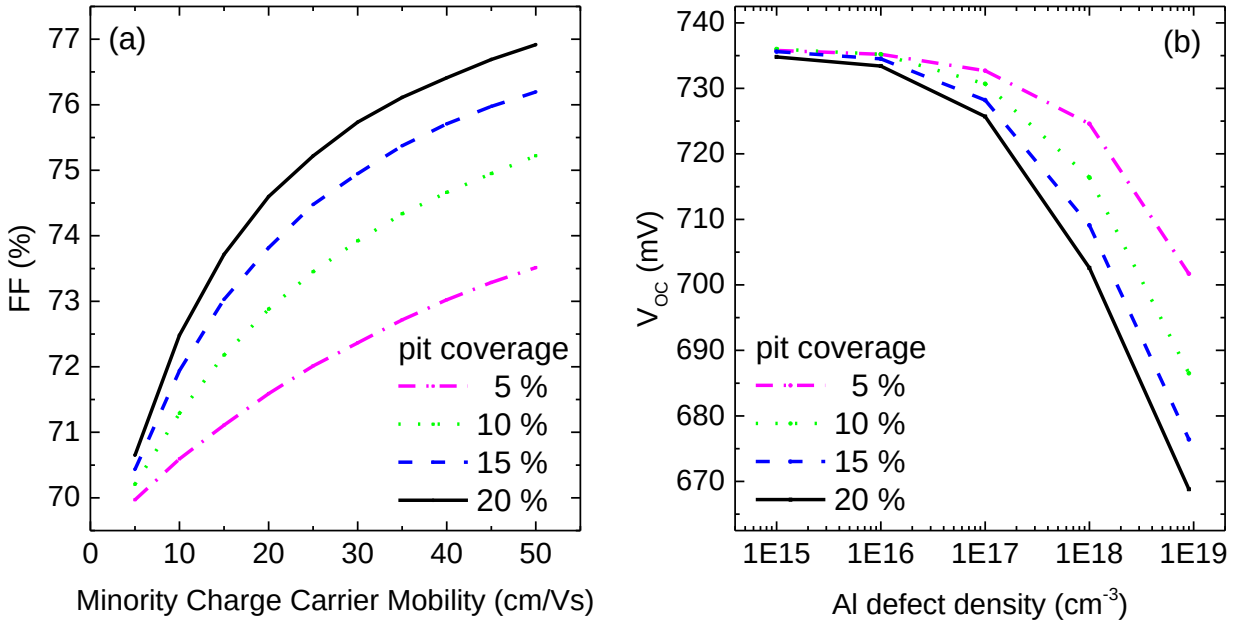

Fig. 6. (Colour online)