



Sinusoidal nanotextures for light management in silicon thin-film solar cells

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Recent progresses in liquid phase crystallization enabled the fabrication of thin wafer quality crystalline silicon layers on low-cost glass substrates enabling conversion efficiencies up to 12.1%. Because of its indirect band gap, a thin silicon absorber layer demands for efficient measures for light management. However, the combination of high quality crystalline silicon and light trapping structures is still a critical issue. Here, we implement hexagonal 750 nm pitched sinusoidal and pillar shaped nanostructures at the sun-facing glass-silicon interface into 10 µm thin liquid phase crystallized silicon thin-film solar cell devices on glass. Both structures are experimentally studied regarding their optical and optoelectronic properties. Reflection losses are reduced over the entire wavelength range outperforming state of the art anti-reflective planar layer systems. In case of the smooth sinusoidal nanostructures these optical achievements are accompanied by an excellent electronic material quality of the silicon absorber layer enabling open circuit voltages above 600 mV and solar cell device performances comparable to the planar reference device. For wavelengths smaller than 400 nm and higher than 700 nm optical achievements are translated into an enhanced quantum efficiency of the solar cell devices. Therefore, sinusoidal nanotextures are a well-balanced compromise between optical enhancement and maintained high electronic silicon material quality which opens a promising route for future optimizations in solar cell designs for silicon thin-film solar cells on glass.

1. Introduction

For silicon thin-film solar cells the technology of directly growing and crystallizing 10 µm thin silicon absorber layers on low-cost substrates¹ became of particular interest when silicon Liquid Phase Crystallization (LPC) replaced Solid Phase Crystallization (SPC) techniques.² During LPC the silicon absorber layer is heated above its melting temperature using an electron or a laser beam which is scanned over the sample. Thus, the silicon film is recrystallized from the melt solidifying into grains that are up to a few centimeters long. Recent progress in LPC enabled solar cell efficiencies up to 12.1 %,³ open-circuit voltages above 650 mV and a silicon material quality comparable to multicrystalline silicon wafers.⁴ Since these current record solar cells feature only basic light trapping and particularly a flat light in-coupling glass-silicon interface their short-current density is still limited below 30 mA/cm² so far.

This paper addresses the challenge of combining high quality silicon absorber layers featuring open-circuit voltages above 600 mV with effective measures for light management. These are required to efficiently couple and trap sun light in

10 µm thin silicon layers and thus, to increase cell efficiencies further. One possibility to enhance the optical path length is to structure the active layer itself by using periodic nanotextures.⁵⁻¹⁰ A suitable technology for implementing periodic nanotextures in LPC silicon devices is nanoimprint lithography in combination with glass superstrates coated with a high-temperature stable sol-gel resist.¹¹ When implementing superstrate patterns with an aspect-ratio of 0.5 and steep texture features into LPC silicon thin-film solar cells Preidel et al. found the electronic material quality to decrease resulting in a reduced quantum efficiency and hence, limited efficiencies, despite their increased incoupling of light. On the other hand, a shallow random texture exhibiting an aspect ratio of about 0.03 lead to electronic solar cell characteristics similar to the planar state of the art device, however, lacking a significant light management effect.¹²

In this study, we fabricate and characterize LPC c-Si films and solar cells with 750 nm pitched periodic sinusoidal or pillar shaped nanotextured glass-silicon interfaces. In the context of the above mentioned extreme model textures of Preidel et al. the aspect ratios of the nanostructures were chosen to lie between 0.03 and 0.5. Accordingly, the sinusoidal texture is chosen due to the lack of for high quality silicon detrimental steep texture features. In addition, optical simulations by Lockau et al. revealed that sinusoidal nanostructures exhibit excellent anti-reflective properties for 10 µm thick silicon absorber layers.¹³ The pillar shaped structure with same

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periodicity but less smooth texture was chosen as comparison because of its promising enhanced incoupling of light on a broad wavelength range.¹⁴ Therefore, the pillar structure serves as a reference for optimized optical properties while the planar stack serves as state of the art reference and represents the optimum electronic material quality case. The sinusoidal structure is intended to combine both, good electronic material quality with enhanced optical properties. The high aspect ratio structure of Preidel et al. serves as upper limit since its for optical properties highly beneficial steep feature sizes do not allow for high quality silicon anymore.¹²

We compare these four types of superstrates for state of the art LPC Silicon thin-film solar cells on glass implemented at the glass-silicon interface: (1) a planar stack ("planar"), (2) a smooth hexagonal sinusoidal structure ("Sine"), (3) a sharp hexagonal pillar shaped structure ("Pillar") and (4) the high aspect ratio square lattice structure of Preidel et al. ("SL"). The different stacks are examined and compared regarding their silicon absorber material quality, their optical as well as optoelectronic properties. In addition, the influence of the structural dimensions on the optical properties is analyzed in more detail. Electronic device characteristics are determined from solar cell test structures in order to estimate their potential benefits for future device designs.

2. Results and discussion

2.1 Material quality

To examine the material quality of 10 μm thick silicon films grown and liquid phase crystallized on nanotextured glass superstrates wet chemical Secco defect etching has been performed in order to uncover line and point defects at the silicon surface. Results are depicted in Fig. 1.

On the sinusoidal nanostructure with an aspect ratio of 0.2 almost no etched defect lines or point defects can be found as shown in Fig. 1(a+c). Nevertheless, the occurrence of line defects resulting from grain boundaries, which are sharply

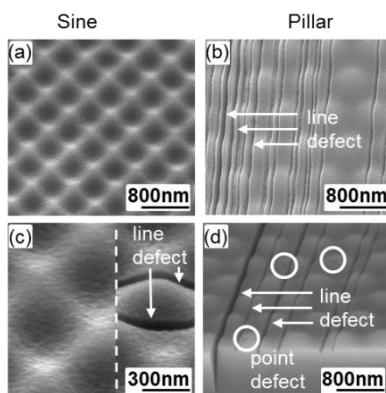


Fig. 1 SEM images of the surface of a 10 μm thick LPC silicon absorber layer grown on (a+c) a sinusoidal or (b+d) on a pillar patterned superstrate after Secco defect etching. (a-c) are top views of the surface and (d) a cross-sectional image tilted by 30°. Some line defects are denoted by arrows, point defects are denoted by circles.

etched (Fig. 1(c)), proofs that defect etching was successful. On the contrary, the silicon absorber layer on top of the pillar structure with an aspect ratio of 0.4 features a high number of line and point defects as shown in Fig. 1(b+d). Hence, these results indicate that the sinusoidal shapes in combination with a lower aspect ratio are favorable for high quality silicon absorber layers being comparable to a respective planar layer (not shown here). The reason for the strongly differing amount of extended defects in LPC silicon layers on sinusoidal and pillar-like textured glasses might be a large number of dislocations that have been shown to occur on steep textures.¹² Thus, a pillar shaped structure with an aspect ratio of 0.4 has already exceeded its upper height limit regarding a high quality silicon growth while for the sinusoidal structures with a maximum aspect ratio of 0.2 this limit has not been reached yet.

2.2 Optical analysis

In order to investigate the impact of the structures' aspect ratio in more detail sinusoidal samples with aspect ratios h/P ranging from 0.09 to 0.25 have been prepared as described in the experimental part. Optical analysis is restricted to the wavelength range of 350 nm to 600 nm since within this wavelength range measurement results of the absorber layers are not superimposed by parasitic absorption in other layers like the glass superstrate. Moreover, the optical properties solely arise from the textured glass-silicon interface since in this wavelength range incident light does not reach the back side of the absorber layer yet and hence, light incoupling properties can be separated from light scattering generated at the back side of the absorber layer. Analysis is done by means of optical spectrometry (Fig. 2).

In general, reflection losses are reduced as the aspect ratio rises. Up to an aspect ratio of 0.15 only a small anti-reflective

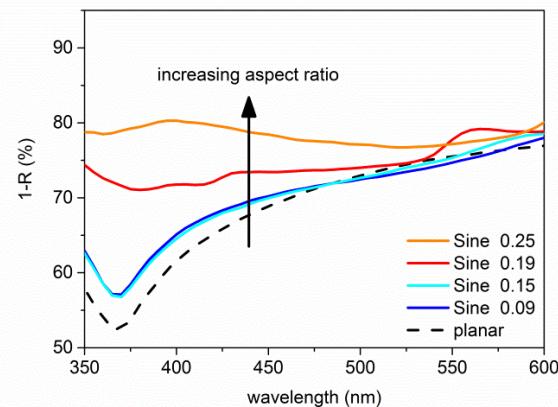


Fig. 2 Optical properties. Absorptance, measured as 1-reflectance (1-R), in the wavelength range between 350 nm and 600 nm for sinusoidal textured 10 μm c-Si absorber layers with varying aspect ratio (numbers are given in the figure according to the colors) are plotted in comparison to a planar reference (black, dashed).

effect and hence increase in absorption is found.

For higher aspect ratios the absorptance increases with increasing aspect ratio. In summary, a 750 nm pitched sinusoidal pattern with an aspect ratio of 0.2 unites both, excellent bulk material quality (paragraph 2.1) as well as superior optical properties (this paragraph), and hence seems to be suited for incorporation into solar cell devices (paragraph 2.3).

2.3 Optoelectronic characterization

For optoelectronic characterization and in order to estimate the photovoltaic performance, solar cell devices have been prepared on a planar reference superstrate as well as on superstrates textured with hexagonal sinusoidal and hexagonal pillar shaped pattern, respectively. For both nanotextures an aspect-ratio of 0.2 has been chosen in order to allow for detailed comparison of the respective properties as independent from structural features as possible. Adapted from the optimized planar stack all devices feature 70 nm SiN_x and 10 nm SiO_x layers at the glass / texture – silicon interface, where the SiN_x provides anti-reflective properties. In this silicon thin-film solar cell device light incidences through the glass-side of the device (superstrate configuration) and metallic contacts are placed on the rear side of the device in order to avoid losses due to shadowing by the grid. Based on these requirements the sinusoidal and pillar shaped nanostructures are implemented at the glass-silicon interface in order to reduce reflection losses of incident light at this interface. In the following, the optical and optoelectronic properties of these devices are analyzed.

Optical reflectance (R) measurements as well as external quantum efficiency measurements (EQE) are plotted in Fig. 3(a). From external quantum efficiency measurements the short-circuit current density (j_{sc}) of a cell can be extracted using

$$j_{sc} = q \int_{300nm}^{1100nm} \Phi(\lambda) \cdot EQE(\lambda) d\lambda$$

where q is the elementary charge of an electron, $\Phi(\lambda)$ the incident photon flux and $EQE(\lambda)$ the measured external quantum efficiency at wavelength λ . Further, these solar cell structures enable the determination of the cell's open-circuit voltage (V_{oc}) using a Suns-Voc measurement setup. Corresponding results are plotted in Fig. 3(b) and 3(c), respectively.

Both sinusoidal and pillar shaped nanotextures exhibit an anti-reflective effect over the entire wavelength range as shown in Fig. 3(a). Reflection losses are reduced by about 5 % (absolute) compared to a planar reference with optimized anti-reflective layer stack. In the wavelength range of 350 nm to 600 nm, where reflection measurements are not influenced by parasitic absorptions in the glass superstrate or other layer stacks at the rear side of the cell device, mean reflectance values are 17.1 % ± 8.8 % for the planar device, 11.0 % ± 3.7 %

for the pillar patterned device and 9.5 % ± 3.0 % for the sinusoidal patterned device, respectively.

When using an additional SiN_x anti-reflective coating the difference between the varied structures becomes smaller. For short wavelength below 600 nm, which means before the light reaches the textured backside of the absorber, the anti-reflective properties of the sine and the pillar structure even outperform the light scattering effect of the higher aspect ratio square lattice structure.

For all devices recombination losses in the electronic device are the cause for the absolute difference between optical and electrical measurements.

Despite the superior optical properties, the external quantum efficiency of the sinusoidal texture (red) cannot outperform the planar reference cell (black, dashed) over the entire wavelength range. For wavelengths smaller than 400 nm the sinusoidal superstrate texture performs better than the planar reference due to an anti-reflective effect. For wavelengths above 750 nm the incident light starts to reach the backside of the 10 μm silicon absorber layer and light is partially reflected back into the absorber layer. This is especially enhanced if the backside of the absorber layer is textured as it is the case for the double-sided textured sinusoidal, pillar (blue) and square lattice (black, points) patterned superstrates. This light trapping effect causes again an enhanced performance of the patterned devices for wavelengths above 700 nm. However, in the wavelength range between 400 nm and 700 nm the external quantum efficiency of the sinusoidal device is reduced. This behavior might be ascribed to a significantly enhanced surface recombination caused by the enlarged surface of the patterned superstrates since no evidence for a disturbed electronic bulk material quality was found during Secco etching. However, compared to the high aspect ratio square lattice device electronic performance could be significantly enhanced which again may be attributed to the superior bulk material quality of silicon being grown and crystallized on the sinusoidal pattern.

The same conclusions as for the sinusoidal pattern can be drawn for the pillar patterned device. However, due to the disturbed material quality of the pillar patterned absorber layers, as it was shown in Fig. 1(b+d), the overall performance of the pillar device is significantly reduced and optical effects start to overcome the electronic disadvantages only for wavelengths larger than about 880 nm. Compared to the high aspect ratio square lattice device a similar performance is achieved. This highlights the importance of the structure's geometry when implemented at the glass-silicon interface. Steep texture features have to be avoided if high quality crystalline silicon material is desired.

This disturbed silicon material quality on the pillar (blue, triangle) and square lattice (black, circle) structure is the reason why short-circuit current densities, shown in Fig. 3(b), and open-circuit voltages, shown in Fig. 3(c), of both structures are significantly lower than for the planar device.

In contrast, sinusoidal nanopatterned cells (red, diamond) exhibit mean j_{sc} values which are comparable to those

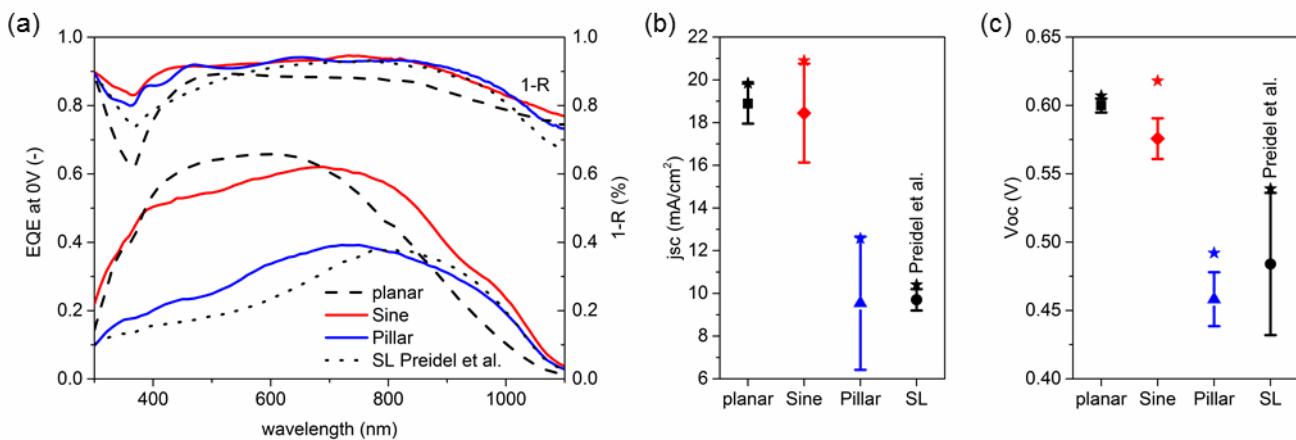


Fig. 3 Opto-electronic properties. (a) External quantum efficiency (EQE) measurements of a planar reference (black, dashed) and sinusoidal (red, aspect ratio 0.2), pillar (blue, aspect ratio 0.2) and high aspect ratio square lattice (black, points, aspect ratio 0.5)¹² patterned devices and corresponding reflectance (R), as $1-R$, are plotted. Averaged cell characteristics (b) short-circuit current density and (c) open-circuit voltages on a planar (black, square), a sinusoidal (red, diamond), a pillar shaped (blue, triangle) and a square lattice (black, circle) structured superstrate are presented. Peak values are denoted by stars.

obtained on planar superstrates and mean V_{oc} values which are slightly lower. It is noteworthy that measurement results of different cells differ more for the textured cells than for the planar cells. Thus, material quality is less uniform on patterned superstrates. While averaged solar cell performance is still slightly lower on sinusoidal textured superstrates, peak values (in Fig. 3 (b+d) denoted by stars) outperform the planar values, in the case of j_{sc} with $20.9 \text{ mA}/\text{cm}^2$ by + 5.3 % (relative) and in case of V_{oc} with 618 mV by + 1.8 % (relative).

Hence, cells on hexagonal sinusoidal nanotextured superstrates have the ability to outperform planar cells if surface recombination losses can be reduced. The passivating and anti-reflective SiO_x and SiN_x intermediate layers have solely been transferred from the optimized planar device and thicknesses have not been adapted for patterned superstrates yet. The successful integration of sinusoidal patterned superstrates into the solar cell devices has proven their suitability for state of the art silicon thin-film solar cell on glass devices and their potential for future improvements in cell design.

3. Experimental

For the hexagonal sinusoidal structure masters were fabricated by Interference Lithography¹⁵ whereas for the pillar structure electron beam lithography was used¹⁶. For comparison, in both cases a pitch of 750 nm was chosen. The structures were transferred onto 1.1 mm thick Corning Eagle XG™ glass superstrates by Nanoimprint Lithography¹⁷ using a high-temperature stable sol-gel resists.¹⁸ For optical analysis

sinusoidal textures with aspect ratios ranging from 0.09 to 0.25 in steps of 0.05 were produced. For optoelectronic analysis both kinds of textures feature an aspect-ratio of 0.2. For material quality analysis a sinusoidal pattern with an aspect-ratio of 0.2 and a pillar pattern of 0.4 as extreme case have been chosen. The structured superstrates were coated with a 250 nm SiO_x -barrier, which inhibits impurity diffusion out of the glass superstrate into the silicon absorber. In case of the pillar structures this barrier was deposited on top of the imprinted structure, in case of the hexagonal sinusoidal structures this barrier was below the imprint in order to prevent flattening of the structures. The superstrates are coated with a layer stack consisting of 70 nm SiN_x and 10 nm SiO_x , where the SiN_x provides an additional state of the art anti-reflection coating for planar devices.¹⁹ On top of all superstrate stacks a 10 μm thick silicon absorber was deposited using electron beam evaporation. The absorber layers were deposited at 600 °C resulting in nanocrystalline material, which is subsequently liquid phase crystallized (LPC) using a laser beam of 808 nm with a scanning speed of 3 mm/s. Before laser crystallization the samples were capped with a 250 nm thick SiO_x -layer resulting in a double-sided textured silicon absorber layer in case a textured superstrate was used.²⁰ Subsequently, the SiO_x -capping layer was removed by wet-chemical etching for nine minutes in a buffered oxide etching solution. On top of these silicon absorber layers solar cells were processed as described in Haschke et al.,⁴ there denoted by test structure, but without final heating step. The fabrication of the square lattice structures can be found in Preidel et al.¹² Fig. 4(a) depicts a schematic sample stack and

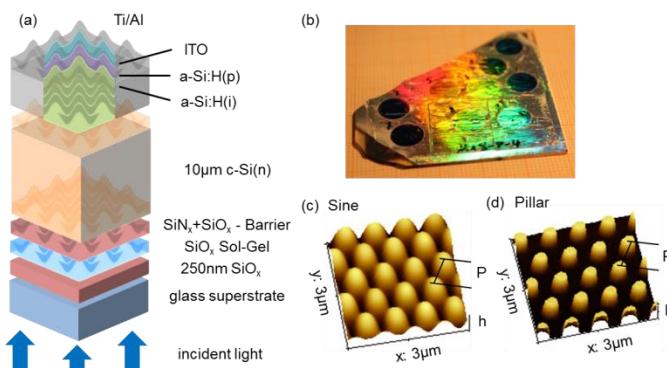


Fig. 4 (a) Schematic and (b) photograph of the solar cell test structure on a sinusoidal patterned glass superstrate. Atomic force microscopy image of (c) sinusoidal and (d) pillar patterned glass substrates. The height (*h*) and the pitch (*P*) of the structures are denoted.

Fig. 4(b) a photograph of the solar cell device. Due to the light scattering effect of the periodic nanotextures samples shimmer colorful under certain angles of incident light. Atomic force microscope images of a sinusoidal and a pillar shaped textured superstrate are shown in Fig. 4(c) and Fig. 4(d), respectively.

Additional sinusoidal samples without SiN_x -film were produced in order to analyze the optical effects resulting from the structure alone without superposition of anti-reflective layer effects. Some of the optical analysis samples were prepared by solid phase crystallization by thermal annealing of amorphous silicon at 600 °C since it is a fast and easy process and optical material properties do not differ from LPC silicon in the wavelength range of interest being well below 900 nm.²¹ Optical characterization was performed using a Perkin Elmer LAMBDA 1050 spectrometer featuring an integrating sphere. Open circuit-voltages (V_{oc}) were obtained by Suns-Voc measurements carried out at room temperature using a Suns-Voc unit of a WCT-100 photoconductance lifetime tool by Sinton Instruments. Short-circuit current densities (j_{sc}) were obtained by external quantum efficiency measurements using a custom-made setup featuring a probe beam size of 3 mm x 2 mm. Height determination of the structures was realized by AFM imaging using a Park Systems XE-70. Material quality was investigated by wet chemical Secco defect etching. Microscopy images were obtained using a Hitachi cold field emitter SEM.

4. Conclusion

We successfully integrated nanoimprinted, high-temperature stable hexagonal 750 nm pitched sinusoidal and pillar shaped structures into 10 μm thin silicon thin-film solar cells. Compared to a planar device with optimized anti-reflective layer stack reflection losses at the glass-silicon interface were reduced over the entire wavelength range by - 5 % (absolute). Compared to a high aspect ratio reference optical benefits could be maintained while the electrical performance was significantly enhanced. Compared to an optimized planar reference device sinusoidal patterned solar cells demonstrated

a higher external quantum efficiency for wavelength being smaller than 400 nm as well as longer than 700 nm due to the anti-reflective effect of the sinusoidal patterned glass superstrate and the light-trapping effect of the double-sided textured absorber layer. Over all a cell performance similar to the planar reference is achieved. Secco defect etching revealed an excellent silicon bulk material quality on the sinusoidal texture being comparable to a planar absorber and enabling open circuit voltages up to 618 mV. Hence, for the sinusoidal pattern surface recombination losses have to be reduced in order transfer the optical achievements into an electrical cell performance enhancement over the entire wavelength range. Peak values of sinusoidal patterned devices already outperform their planar references in terms of V_{oc} and j_{sc} demonstrating that sinusoidal patterned substrates are promising candidates for future cell designs for silicon thin-film solar cells on glass.

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