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RESEARCH ARTICLE

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Double-sided nano-textured surfaces for industry compatible high-performance silicon heterojunction and perovskite/silicon tandem solar cells

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Abstract

Nano-textured surfaces are an intriguing approach for optimizing the optical characteristics for monolithic perovskite/silicon tandem solar cells. Here, the development of different textures of silicon surfaces using various commercial additives is presented and their performance in silicon heterojunction (SHJ) and SHJ–perovskite tandem solar cells is discussed. After optical and electrical characterization, we show that nano-textured surfaces can easily compete with standard textured surfaces, yielding higher average efficiencies in single junctions. In addition, their compatibility with solution-processed perovskite top cells is demonstrated, yielding a perovskite/silicon tandem solar cell efficiency of >28% on a bottom cell with nano-texture on both sides.

KEYWORDS
anisotropic surface etching, nano-textured silicon, passivating and carrier-selective contacts, perovskite/silicon tandem solar cells, SHJ

1 | INTRODUCTION

For many solar cell types, optimizing light in-coupling by textured surfaces is not compatible with electronically optimal growth of subsequent layers on top of the textured surface. Therefore, nano-textured silicon surfaces became an appealing approach to enhance light trapping in the silicon bottom cell absorber for metal-halide perovskite/silicon tandem solar cells.[1,2] Moreover, in commercially available silicon heterojunction (SHJ) solar cells, nano-textured surfaces might also have the potential to replace standard textured surfaces that normally feature random pyramids with heights in the range of 1–5 µm. Especially for cell production, where the expenses for the silicon wafer represent the highest cost factor in production,[3] a reduction in silicon loss due to lower etching abrasion of the wafer could be an interesting option to reduce costs. Since the texture not only is crucial to enhance light trapping but also has a high impact on the surface defect density, electrical properties of the c-Si wafers, such as the lifetime of the minority charge carriers, are influenced as well. It was shown previously that a reduced pyramid size still results in excellent passivation and minority carrier lifetimes.[4,5]

To allow the wet processing of the perovskite absorber, which normally has a thickness of 0.5–1 µm, the pyramid height must be well below 1 µm to prevent the generation of local defects or shunts in the top cell.[1,4] Different methods can be used for the deposition of

the perovskite film, such as blade- or slot-die coating, physical vapor deposition, or spin coating. Until now, the latter is the most successful technique at lab scale, providing high film quality on flat surfaces as well as on mild textures.[6–8] For example, Hou et al.[6] combined a mild silicon texture with pyramid heights around 2 µm with a solution-processed wide-band gap perovskite layer in the micrometer range yielding 25.7% power conversion efficiency in a perovskite-textured SHJ tandem solar cell. Recently, the KAUST group even reported a 29.3% efficient tandem cell by wet processing on mild Si texture.[9] Sahli et al.[10] reported on a top cell deposition process on standard textured surfaces. A conformal coating of this Si texture was obtained by using evaporation and a solution-based hybrid process reaching an efficiency of 25.2%. Recently, the EPFL group improved it to 29.2%.[11]

To yield nano-textured Si surfaces, different approaches have been published. Most commonly, such textures are obtained by anisotropic surface etching[1,4] but, as recently shown, also by nano-imprint lithography, where reactive ion etching combined with wet chemical etching yields sinusoidal nanostructures with adjustable heights.[12] However, etching in alkaline solution with KOH or NaOH is the most relevant to industry, being a cost-efficient and well-established process.[13] Moreover, the nano-texturing process presented in this paper enables a leaner production of the bottom cell for perovskite/silicon tandem solar cells, since to produce the front polished and textured rear side, multiple additional processes would be necessary.

The optical characteristics of a pyramid-textured surface and hence their impact on the solar cell performance strongly depend on different parameters like pyramid density, height, and homogeneity.[14] To decrease pyramid height, different approaches are possible, such as decreasing etching time, increasing KOH concentration, or adding an increased amount of isopropyl alcohol (IPA) to the etching bath.[15] However, these processes often do not ensure a very uniform texture but show a broad pyramid-height distribution. One important reason for such an inhomogeneous etching result is the development of H_2 during the etching process.[14,16] Namely, in a redox reaction, silicon reacts with KOH in the presence of water as follows:

$$Si + 2KOH + H_2O \rightarrow K_2SiO_3 + 2H_2 \quad (1)$$

The gaseous hydrogen reaction product aggregates to bubbles of different sizes that act as pseudo-masks on the hydrophobic silicon surface, retarding the etching process at some points on the wafers, which disturbs a uniform transport of reactants and products from the silicon surface. This leads to inhomogeneous initiation of the etching reaction on the surface and, consequently, to different pyramid densities and heights. The more hydrophobic the silicon surface, the bigger the H_2 bubbles and the bigger the pyramids after etching.[14,16]

To avoid such inhomogeneous results, surface-active chemicals are used as additives during etching. It was shown that using IPA, the wettability of the surface was increased[17] and, hence, H_2 bubbles were avoided, yielding a higher homogeneity of the textured surface. The pyramid heights depend also on the etching rate, that is, the amount of etched material over time. The higher the etching rate, the larger the resulting pyramid height. Counter-intuitively, by adding more KOH, the etching rate slows down due to a self-liming etching process at the Si surface, leading to the formation of smaller pyramids. Etching small pyramids in such way, however, holds the chance of an incomplete coverage of the surface by the pyramid texture.[15,18] Another possibility to influence the etching rate is adding other additives, such as potassium silicate (K_2SiO_3) or sodium silicate (Na_2SiO_3). It was shown in[4] that the addition of K_2SiO_3 slows down the etching rate and ensures improved control of growth and nucleation kinetics. Following Equation (1), the equilibrium of the reaction is shifted to the educts, which leads to slower etching. This can be seen in the decrease in pyramid height when adding more K_2SiO_3.[4]

To yield excellent performance in solar cells, nano-textured surfaces must show low reflectivity, for which it is crucial to ensure the complete coverage with pyramids with a uniform pyramid height. Therefore, although the pyramid height can be adjusted by the concentration of KOH and silicate in the etching solution, many published studies use commercially available surface-active additives. The exact composition of such additives mostly remains undisclosed, which makes it difficult to unravel the chemical processes involved. Nevertheless, since these have surfactant components, they are of great importance for good surface wetting during the etching process.

In this work, we investigate three different texture processes (A, B, and C), which all contain different commercially available additives. First, the texture process A for nano-textures is shown, containing an anionic surfactant as an additive. Furthermore, texture processes B and C are investigated in detail, of which the latter is split in processes C.1 and C.2 for nano-textures and standard micro-textures, respectively. In addition, we show the impact of the silicon absorber material using industrial Cz material from two different suppliers.

Results of SHJ solar cells with nano-textures on both sides are shown, emphasizing their superior performance compared to cells with standard texture. In addition, initial results with such silicon bottom cells used in perovskite/silicon tandem solar cells with a spin-coated top cell reached an efficiency of 28.4%. This offers an industrially more easily applicable alternative to the single-side textured bottom cells presently used for the best lab cells and a performance improvement compared to the single-side chemically polished Cz-Si-based bottom cells that were shown by Köhnen et al.[19] Using an only 100-µm-thick Cz wafer with standard random pyramids on the rear and a chemically polished front, they reached 27.9%, limited by a low current density of 17.8 mA/cm^2 of the bottom cell.

2 | EXPERIMENTAL SECTION

2.1 | Nano-textured silicon surfaces by anisotropic etching in KOH solution

For the development of the nano-texture, different (<100>) n-type Cz-silicon wafer types were used from two different suppliers. For the

initial development of the nano-texture with texture process A, wafers with an initial thickness of 150 µm and 5 Ω·cm base resistivity (type X) were used. For testing the micro-texturing and for the comparison of the different texture processes A, B, and C in SHJ solar cells, type X wafers with a thinner initial thickness of 130 µm and 5 Ω·cm base resistivity have been employed. In addition, wafers from another supplier (type Y) were used, which had an initial thickness of 160 µm and a resistivity of 1.2 Ω·cm.

First, all samples have been subjected to a standard saw damage etching (SDE) step with high KOH concentration at 90 °C.

The subsequent texturing step was carried out in an alkaline solution consisting of DI water, KOH, K_2SiO_3, and a commercial additive at 75 °C. Three different additives were used, in the following referred to as texturing processes A, B, and C. Since for our standard texturing process for micro-pyramids the same commercial additive is used as in the process C, we denote the process for nano-textures "C.1" and for micro-textures "C.2." The texturing process C.2 for the standard micro-texture contains DI water, KOH, and the commercial additive C. It is carried out at slightly higher KOH volume fraction, at lower additive concentration, and at a higher temperature (80 °C) with a texturing time of 8 min.

First, we developed texturing process A. Here, we investigated the influence of the ratio of concentration $F = \mathrm{KOH}/K_2SiO_3$, the etching time, and the concentration of the commercial additive on the pyramid structure. Having optimized texture process A in an extensive parameters study in terms of a promising process for tandem solar cells applications, namely, small pyramid height (<1 µm) and low standard deviation, we then applied the commercial additives B and C with the same parameters, to investigate the impact on the texture. Here, we assumed that the variation of the additive will not drastically change the picture and will not require a complete re-optimization of the process. The focus of this work, however, is not to find the best additive but to correlate the wafer texture with solar cell performance. After the texturing step, all samples were cleaned by an RCA final cleaning procedure. The different textures were characterized by scanning electron microscopy (SEM) imaging. An in-house developed software tool was used to determine the distribution of pyramid heights.

Optical reflectivity was measured by using a Perkin Elmer Lambda 1050 spectrophotometer in the wavelength range 250–1200 nm.

2.2 | Integration in solar cells

A. Silicon heterojunction solar cells

To investigate the impact on device performance, we integrated differently textured wafers in rear-junction, bifacial SHJ solar cells. We used wafers X, having an initial thickness of 130 µm and a base resistivity of 5 Ω·cm, for all the texturing processes. In addition, for texturing process A, a set of samples on the 160-µm-thick wafers of type Y with a resistivity of 1.2 Ω·cm were used.

For the solar cells, the a-Si:H(i)/nc-Si:H(n) layer stack on the front side (29 nm on flat) and the a-Si:H(i)/a-Si:H(p) layer stack on the rear side (18 nm on flat) were deposited using plasma-enhanced chemical vapor deposition (PECVD) in an Applied Materials AKT1600 cluster tool.

After PECVD, lifetime measurements were carried out using a Sinton Instruments WCT-120 lifetime tester in transient mode. J_0 is determined by fitting the lifetime as a function of the injection density Δn for $\Delta n > 10^{15}\ \mathrm{cm}^{-3}$ ($T = 300$ K).[18] Photoluminescence (PL) imaging was measured using an in-house developed tool.

Transparent conducting oxide (TCO) layers (99% indium oxide from newSCOT target from ANP Corp.) were deposited by DC sputtering on the front with a thickness of 110 nm (on flat) and on the rear with 55 nm. The solar cell area was defined using aligned sputter masks on both sides of the wafer with a cell area of 4 cm^2. Finally, the front and rear metallization with grids was done by screen printing of a low-temperature silver paste. On the front, the grids exhibit 12 fingers and on the rear 25 fingers. After screen printing, all samples were annealed at 210 °C for 10 min under ambient air and subsequently light-soaked at 210 °C under 1 sun illumination for 5 min.

B. Perovskite/silicon tandem solar cells

To reduce reflection losses and hence to increase the short-circuit current density[20] in the perovskite/silicon tandem solar cell, bottom cells with a nano-textured surface featuring pyramids with an average height of 500 nm (texture process A, wafer type Y) were used (initial silicon wafer thickness of ∼180 µm, after texturing ∼160 µm). Compared to the SHJ cell processing as described above, the front side was modified to facilitate an ideal opto-electrical coupling to the top cell; namely, the nc-Si:H(n) layer was replaced by a ∼90-nm (on flat) thick nc-SiO_x(n) layer. On a flat front surface, the optically ideal thickness was found to be 110 nm (on flat) with a refractive index of 2.6.[21] For forming contacts on both sides of the wafer, the same TCO as for SHJ single junction cells was used. A stack of TCO (180 nm on flat)/Ag (400 nm on flat) was sputtered on the rear and 20 nm (on flat) TCO was sputtered on the front, defining the cell area of ∼1 cm^2 by aligned sputter masks on both sides. The top cell was then fabricated, similarly to the top cell presented by Al-Ashouri et al.[22] First, the hole transporting material (self-assembled monolayer Me-4PACz) was spin-coated (3000 rpm, 30 s) and annealed at 100 °C for 10 min. A wide-band gap (1.68 eV) perovskite absorber layer ($Cs_{0.5}(MA_{0.17}FA_{0.83})_{0.95}Pb(I_{0.83}Br_{0.17})_3$) was subsequently deposited by spin coating (3500 rpm, 5-s acceleration, 35 s) and annealed on a hot plate at 100 °C for 20 min.

A LiF passivation layer (1 nm) and C_{60} as the electron transport layer (18 nm) were thermally evaporated. A SnO_2 buffer layer was then deposited by thermal atomic-layer deposition (ALD) using TDMASn as a precursor and water as oxidant. Then, an indium zinc oxide (IZO)-based front electrode (100 nm) was RF sputtered in a lab system, and a silver ring for electrical contacting

outside of the active cell area was thermally evaporated. Finally, LiF (100 nm) was evaporated and serves as an anti-reflection (AR) coating.

C. Characterization

The current–voltage (*JV*) characteristics of the cells were measured under standard test conditions (AM1.5G; 25 °C) (class AAA) with shadow masks to define the illuminated area being 4 cm^2 for SHJ and 1 cm^2 for tandem cells. External quantum efficiency (EQE) measurements were performed without optical losses from the front grid using a home-built system, equipped with Xenon and Helium lamps. To measure the two tandem sub-cells separately, the cells are illuminated by a chopped monochromatic probe beam (78 Hz) and a continuous wave (CW) bias light with different wavelengths leading to a limitation of the sub-cells depending on the applied bias light. Hence, by applying a defined bias-voltage, it is possible to measure the two sub-cells at their short-circuit current condition. Reflection measurements were performed using a spectrophotometer (Perkin Elmer UV–Vis Lambda 1050) in the range of 250–1200 nm.

3 | RESULTS

3.1 | Nano-textured silicon surfaces by anisotropic etching in KOH solution

For optimizing the nano-texture, we first adjusted the volume fraction φ_A of the commercial additive in the texturing process A, while keeping the volume fraction of KOH and K_2SiO_3 constant. Figure 1 displays SEM images of Cz silicon surfaces etched with three different volume fractions: $\varphi_A = 1.07{\cdot}10^{-2}$, $1.17{\cdot}10^{-2}$, and $1.27{\cdot}10^{-2}$.

The resulting topography clearly emphasizes the critical dosing of the commercial additive for homogeneous pyramid formation (cf. Figure 1). Both too low ($\varphi_A = 1.07{\cdot}10^{-2}$) and too high ($\varphi_A = 1.27{\cdot}10^{-2}$) volume fractions result in a large fraction of flat areas, which will increase reflection and reduce the ability to couple light into the Si wafer and, potentially, will lead to a more inhomogeneous passivation layer thickness. A medium volume fraction of $1.17{\cdot}10^{-2}$ is found to be optimal for a good wetting during etching and, hence, a high coverage with pyramids.

Therefore, for the rest of the experiment, this commercial additive in process A was used with a constant volume fraction of $\varphi_A = 1.17{\cdot}10^{-2}$. In the next steps, we addressed the optimization of the ratio of volume fractions $F = K_2SiO_3/KOH$ and its impact on pyramid height, pyramid density, and reflectivity. Figure 2 shows SEM images of the texture achieved by etching with different ratios $F = 0.4$, 1.0, 1.4 and without the addition of any K_2SiO_3 ($F = 0$). Our standard micro-textured surface (later on referred to as texturing process C.2) is shown for reference. In addition, the height distribution of pyramids is displayed in Figure 2.

Increasing *F*, that is, by increasing the K_2SiO_3 volume fraction, the pyramid density increases and the average pyramid height decreases. Adding the same amount of K_2SiO_3 as KOH, the pyramid density increases by a factor of 1.8 compared to etching without K_2SiO_3. The average height decreases with increasing K_2SiO_3 fraction, resulting in a nano-textured surface with an average height of 0.50 µm at $F = 1.0$, being further reduced to 0.44 µm at $F = 1.4$. The latter two samples exhibit a narrow distribution as indicated by the interquartile ranges shown in Figure 2.

Whereas for the micro-texture, only 24% of the pyramids are below 1-µm height, for the adapted process shown in Figure 2 ($F = 0$), the fraction increased up to 77%. The addition of K_2SiO_3 further increases the proportion to over 90% with up to 98.8% for $F = 1.4$. This is especially important for their application as bottom cells. Moreover, the impact of the different textures on optical losses is investigated. For that end, reflectivity measurements were carried out on these different nano-textures, as well as on the standard micro-textured surface, and on a polished Si surface for reference.

As shown in Figure 3, the impact of the texture is visible all over the relevant wavelength range of 400–1100 nm. The impact of *F* can most clearly be seen at wavelengths around 1000 nm where reflectivity clearly increases with increasing *F*. Interestingly, the micro-textured surface shows a similar reflection as the one with $F = 0.4$

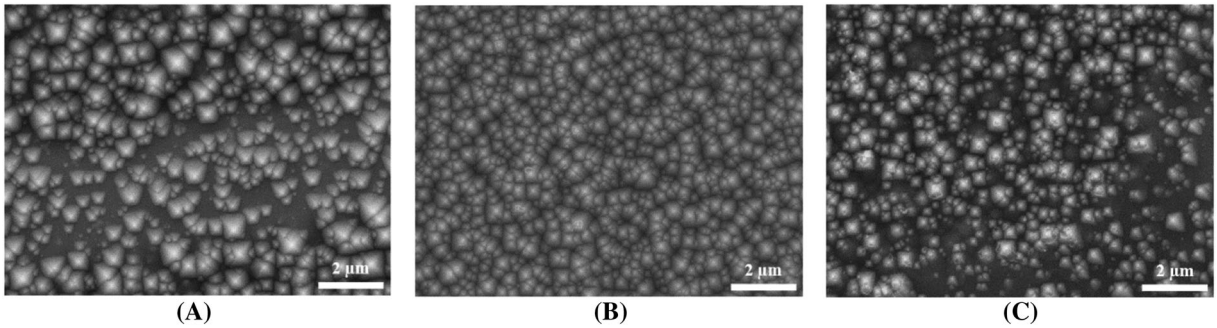


FIGURE 1 Scanning electron microscopy images of silicon surfaces etched in alkaline KOH solution with constant KOH and K_2SiO_3 volume fraction at 75 °C. The volume fraction of the additive A was $\varphi_A = 1.07{\cdot}10^{-2}$ (A), $1.17{\cdot}10^{-2}$ (B), $1.27{\cdot}10^{-2}$ (C), and $F = KOH/K_2SiO_3 = 1.4$.

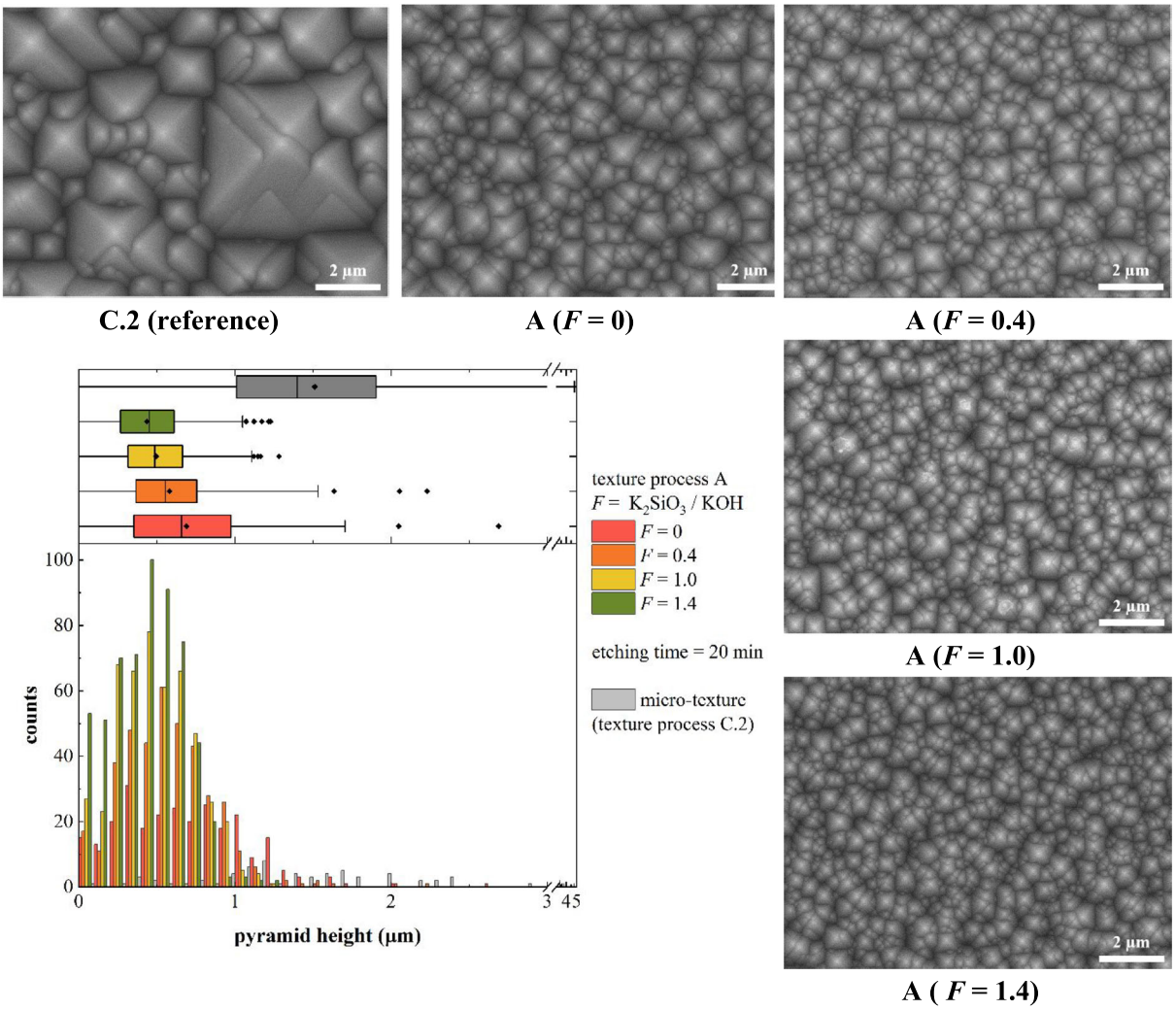


FIGURE 2 Histograms of the pyramid heights and interquartile ranges of the distributions (above) of a standard micro-textured surface (C.2 = reference) and surfaces etched with different ratios *F* but constant volume fraction of the additive A $\varphi_A = 1.17{\cdot}10^{-2}$ and their corresponding scanning electron microscopy images. All samples were etched for 20 min at 75 °C.

and, in the near-infrared (NIR) range, even slightly higher reflection than samples etched without the addition of K_2SiO_3 ($F = 0$).

In contrast, the sample with $F = 1.4$ shows an overall higher reflection with a deviation of 2.4% (abs) at 1000 nm compared to a micro-textured surface. Surfaces etched with $F = 1.0$ exhibit an increase by only 1.4% (abs). Increasing the median pyramid height to 550 nm ($F = 0.4$) leads to a further reduction by 1% compared to $F = 1.0$. This shows that nano-textures exhibit reasonably low reflectivity when measuring directly on the silicon wafer, and reflectivity can become (almost) as low as for a standard textured surface. On the one hand, reflection increases with decreasing pyramid size due to the fact that the range of the wavelength of the incoming light is reached, and hence, geometric optics is hindered. This is obvious from the series ($F = 0$, ..., 1.4). On the other hand, a more homogeneous and more narrow distributed pyramid size apparently helps to decrease reflection. This is obvious from the samples C.2 (micro-textured surface) versus A ($F = 0$). Hence, a combination of both a homogeneously, narrow distribution and sub-micrometer sized pyramid texture (A; $F = 0.4$) can compete with standard large, but inhomogeneously distributed, pyramids (C.2).

The ratio *F* clearly impacts the etching rate. While the micro-texture is etched at a rate of 0.4 µm/min, it is only 0.05 µm/min in case of $F = 1.4$. Although having longer etching times for nano-textures than for micro-textures, the removed Si thickness can be reduced by more than 70%; that is, for $F = 1.4$, only 1.9 µm was removed. This allows to use thinner wafers if the aim is a certain final thickness, or if using the same starting material, this will lead to an increased final wafer thickness and hence a better NIR response.

Since for $F = 1.0$ yields an average height of the pyramids (490 nm) with a fraction of pyramids that are below 1-µm height of 98%, and in addition, reflection was still very low, we decided in the next step to stick to this ratio, that is, K_2SiO_3 volume fraction, keeping all other parameters constant but exchanging the commercial additive, while always using the same volume fraction of $\varphi = 1.17{\cdot}10^{-2}$.

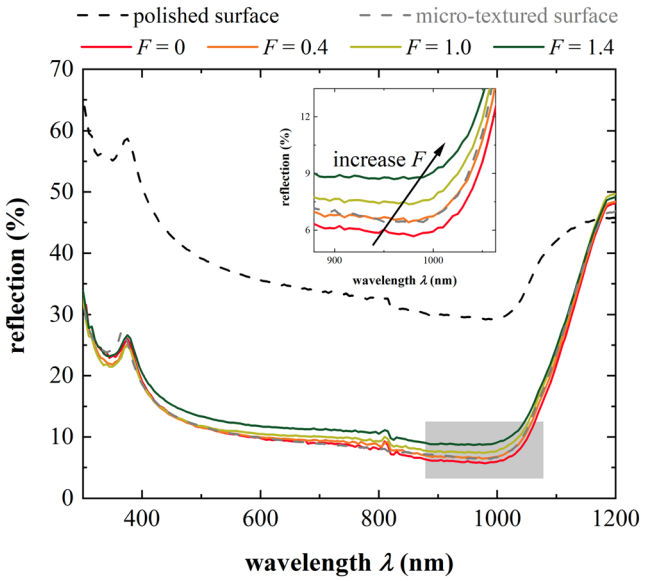


FIGURE 3 Reflection measurements on different textures measured directly on the silicon wafer.

The samples characteristics of the texture processes A–C.2 are shown in Table 1 for both wafer types, X and Y.

The type of additive has a pronounced impact on both etching rate and the median pyramid height. Texture process A yields the lowest etching rates, the smallest average pyramid height, and the highest pyramid densities. Whereas during etching in texture process A, only ~3 µm of silicon was removed, processes B and C.1 lead to a removal of ~8 and >9 µm, respectively. The additive used for texture process A seems to best unblock the surface; hence, the etching process starts on more spots at the same time, resulting in the increased pyramid density and a narrow height distribution. In general, a decrease in pyramid height goes along with an increasing pyramid density on the wafer surface. The distribution of the pyramid height broadens strongly for texture processes B, C.1, and C.2, which renders these processes unsuitable for bottom cells in perovskite/silicon tandem solar cells. Moreover, by comparing the result of the same etching process applied to Cz silicon wafers from different suppliers (cf. Table 1; cf. texture process A for wafer types X and Y), it becomes obvious that the specific silicon surface properties (most likely from a different sawing process) influence the resulting morphology as well.

Next, the samples shown in Table 1 were passivated with a stack of a-Si:H(i)/nc-Si:H(n) on the front and a-Si:H(i)/a-Si:H(p) on the rear as for SHJ cells. Figure 4 shows the implied open-circuit voltages iV_{OC} as derived from quasi-steady-state photoconductance (QSSPC) measurements on nine samples per group (six for process C.2) and injection-dependent minority carrier lifetime curves, each representing a sample with an average performance within the group.

The samples revealed significant differences in the iV_{OC} values after passivation. First, we compare the texturing processes on wafer type X. Process B, yielding the largest pyramids of all nano-textured samples, resulted in the highest values. Processes A and C.1, both with smaller pyramids, lead to slightly worse passivation quality. The standard micro-texture yields comparable iV_{OC} values as process C.1. Lifetime curves of all nano-textured samples are comparable, reaching up to 4.7 ms at $\Delta n = 10^{15}/cm^3$, whereas the standard micro-textured sample shows a lifetime of only 3 ms on average. The highest lifetime value of 5.7 ms (not shown here) was achieved with process B, followed by processes A (5.6 ms), C.1 (5.4 ms), and C.2 (4.0 ms).

Comparing nano-texture and micro-texture, the importance of the surface topography becomes apparent. Keeping in mind that volume recombination and surface recombination coexist, and the bulk recombination should be comparable for all wafers of the same type and from the same batch, it is most likely that the difference in lifetime is due to the different surface recombination velocities. Therefore, we propose that nano-textures lead to lower surface recombination, hence higher lifetimes.

Comparing wafer types X and Y, the lower resistivity (and larger thickness) of type Y wafers comes with higher bulk recombination, which is reflected in a lower iV_{OC} and a lower lifetime, in particular for low injection (2.5 ms vs. 4.2 ms at $\Delta n = 10^{15}/cm^3$), as can be seen in Figure 4B. In addition, not shown here, type Y wafers yield the highest saturation current densities J_{0e} in solar cells, which also correlates with lower lifetimes.

3.2 | Solar cells

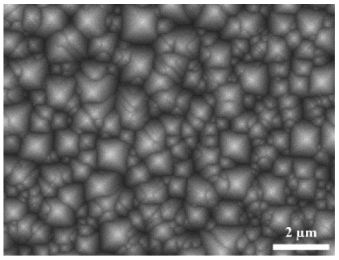
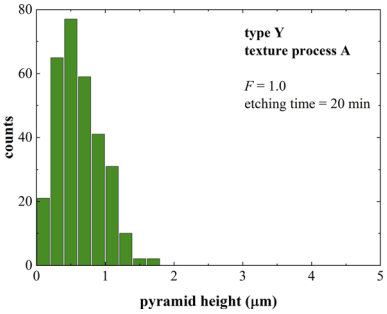
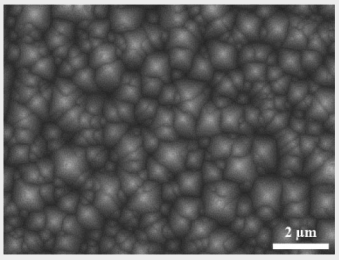
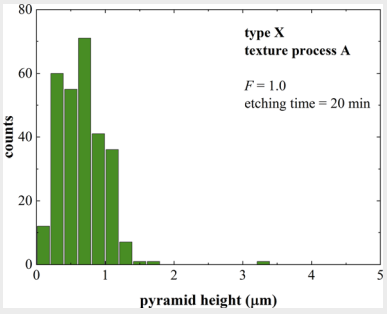
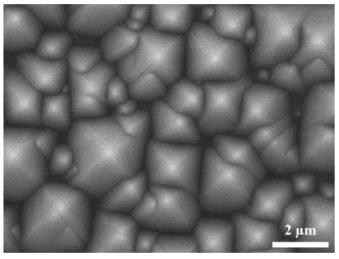
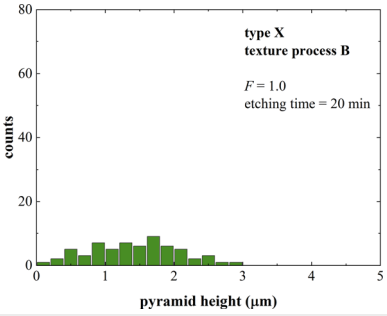
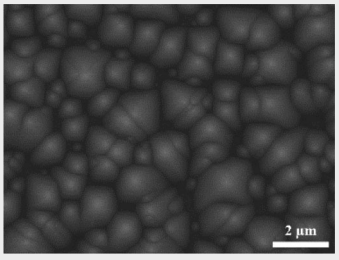
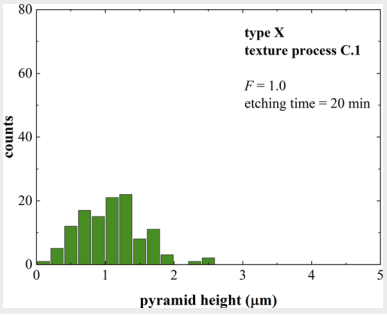
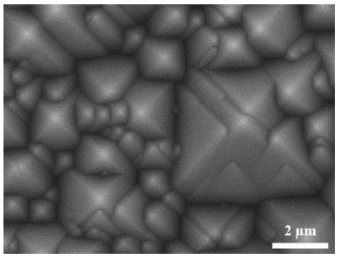
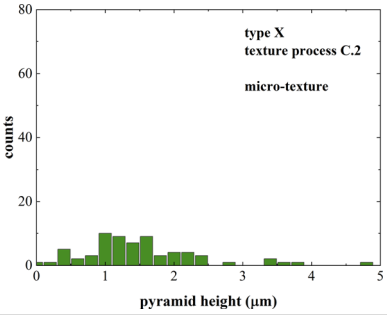
A. Silicon heterojunction solar cells

Wafers with the different texture processes A, B, C.1, and C.2 were used for SHJ solar cells. Figure 5 shows the cell parameters as determined from the *JV* curves. The short-circuit current density J_{SC}, the open-circuit voltage V_{OC}, the fill factor *FF*, and the power conversion efficiency η are shown for all texture processes.

As expected from the lifetime measurements, type Y wafers yield cells with the lowest V_{OC}, with a median of 739.2 mV being in average 4 mV smaller than for cells on type X wafers. Not only is lifetime lower for type Y, but also recall that the wafer is thicker by ~20 µm, which explains the higher J_{SC}. However, iV_{OC} values after PECVD and V_{OC} values of the solar cells do not match for every group, which indicates that the different surfaces not only result in different passivation but also react differently to the subsequent processes, such as sputtering and screen printing. Comparing the two suppliers, type Y reached high *pFF* of 85.2% compared to type X with 84.3%. This is also visible in the *FF*, where the difference is even larger due to a lower series resistance of cells fabricated on type Y wafers (0.7 Ω·cm^2 vs. 0.8 Ω·cm^2). In the end, the higher values for J_{SC} and in particular *FF* overcompensate the lower V_{OC}, resulting in the highest efficiency on type Y material (η = 23.7% median).

Comparing in the following type X nano-textures with the standard micro-texture process C.2, it can clearly be seen that the nano-textures can easily compete with a micro-texture. Interestingly, texture processes A and B yield higher J_{SC}, with 39.1 and 39.2 mA/cm^2 (median), respectively, compared to C.1 (38.8 mA/cm^2) and C.2

TABLE 1 Characteristics of samples etched with different commercial additives.

Sample	SEM image	Histogram of pyramid heights	Etching rate (µm/min) Median height (µm) Pyramid density (µm^{-2}) Removed thickness (µm) Final thickness (µm)
Wafer type Y Texture process A			0.07 0.58 2.9 2.7 140
Wafer type X Texture process A			0.08 0.65 2.6 3.1 ~110
Wafer type X Texture process B			0.20 1.50 0.6 8.0 ~105
Wafer type X Texture process C.1			0.25 1.12 1.2 9.8 ~105
Wafer type X Texture process C.2			0.40 1.40 0.6 6.8 ~110

Abbreviation: SEM, scanning electron microscopy.

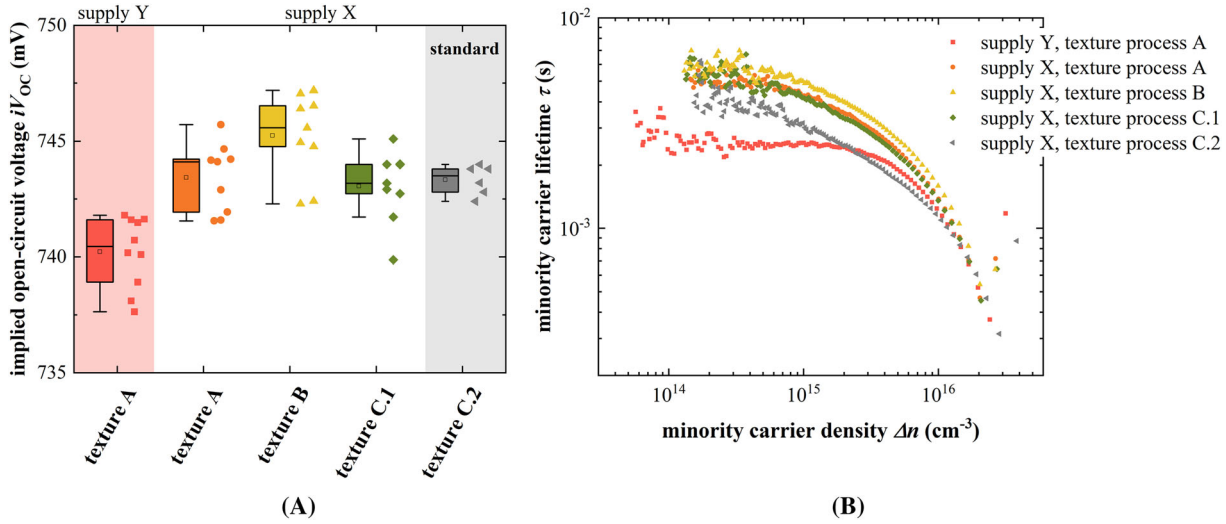


FIGURE 4 Quasi-steady-state photoconductance measurements after plasma-enhanced chemical vapor deposition in transient mode of the (A) implied open-circuit voltage iV_{OC} and (B) injection-dependent lifetime representing the average per group of nano-textured and standard micro-textured surfaces.

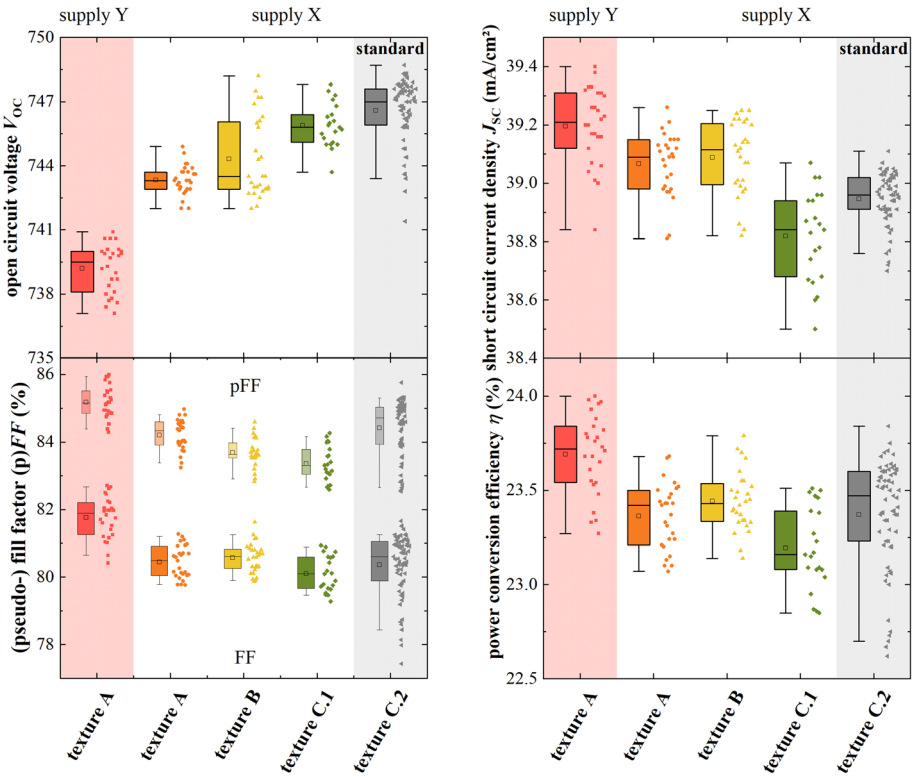


FIGURE 5 *JV* parameters of silicon heterojunction solar cells based on wafers (suppliers X and Y) with different texture processes.

(39.0 mA/cm^2). Although the micro-texture tends to have the highest *pFF*, processes A, B, and C.2 result in comparable *FF* and achieve efficiencies in the same range. The (median) efficiencies are as follows: $\eta_A = 23.4\%$, $\eta_B = 23.4\%$, $\eta_{C.1} = 23.2\%$, and $\eta_{C.2} = 23.5\%$. The highest efficiency was measured on type Y material after texture process A with $\eta = 24.0\%$, $FF = 82.5\%$, $V_{OC} = 740.6$ mV, and $J_{SC} = 39.3$ mA/cm^2 mostly due to the higher (*p*)*FF*.

Figure 6 shows both EQE and total reflection measurements of samples with texture processes A (types X and Y) and C.2 (type X), using the same color code as above. The current density J_{EQE}, as calculated from the EQE curves, and the current loss $J_{(1-R)}$, as calculated from the reflection measurements $(1 - R)$, are listed. Comparing the cells on type X material first, the current loss due to reflection is the lowest for micro-textured surfaces. Nano-textures, in contrast, show a

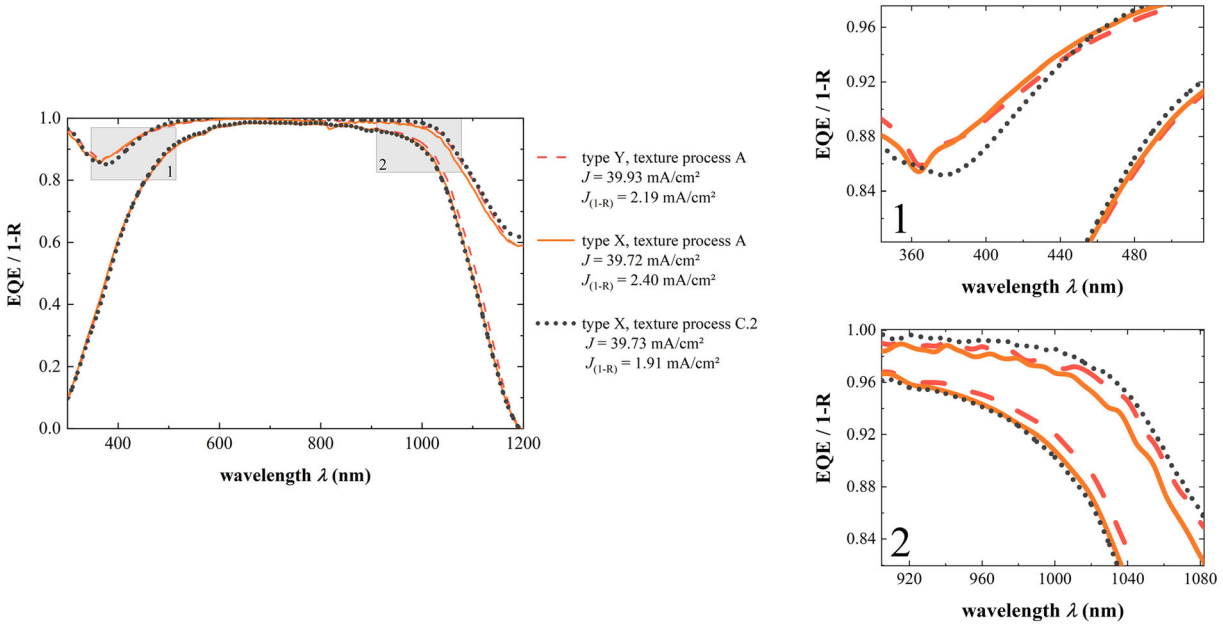


FIGURE 6 External quantum efficiency (EQE) and reflection results of silicon heterojunction solar cells measured with grid shading.

loss being higher by 0.3–0.5 mA/cm^2 as could be expected from the reflectivity on the wafers (Figure 3). Whereas texture process B shows almost the same behavior as C.2, texture process C.1 shows an overall lower EQE in the range of 500–900 nm (B and C.1 not shown here). Despite the higher reflectivity, the nano-textures do not show a significant difference in EQE in the NIR range compared to the micro-texture. In the short wavelength range, both textures perform similarly.

Next, the results of the (20 nm thicker) type Y wafer are compared to those of type X wafer, both with the same texture process A. For type Y wafers, a small loss at short wavelengths is overcompensated by the increased EQE in the NIR range (800–1200 nm), leading to an overall gain of 0.2 mA/cm^2, resulting in the highest value of $J_{EQE} = 39.9$ mA/cm^2. The gain in the NIR range is expected and ascribed to the thicker wafer.

In conclusion, nano-textures do not lead to a loss in current and exhibit high *pFF*, resulting in high efficiencies. All *JV* parameters were similar or even slightly better as compared to those of cells with our standard micro-texture C.2. In particular, the potential current density loss in the NIR range, most relevant for the application as bottom cells in tandems, is very low.

B. Perovskite/silicon tandem solar cells

To demonstrate their high potential as bottom cells, we processed perovskite/silicon tandems using monofacial SHJ cells on type Y wafers using texture process A for both sides. A monofacial SHJ cell using float zone material (~260-µm Si thickness) featuring a polished front and a micro-textured rear side, as usually used in our best tandem cells, serves as reference. For the top cell, a similar process was used as that presented by Al-Ashouri et al.[22] Despite the textured surface of the bottom cell, spin coating of the self-assembled monolayer (hole transporting material) and the perovskite absorber was achieved with complete coverage of the nano-pyramids.

The *JV* scans and the *JV* results from maximum power point (MPP) tracking of the best tandem devices are shown in Figure 7A. A power conversion efficiency of 28.4% is reached with nano-texture. The EQE presented in Figure 7B shows that the sub-cells of the tandem device are not in current matching condition (with sub-cell current densities of 19.8 mA/cm^2 for the top cell and 19.0 mA/cm^2 for the bottom cell). The bottom cell current density is higher as compared to the chemically polished front and micro-textured rear Cz-Si-based bottom cell, as was presented in,[19] yielding 17.81 mA/cm^2. This is not only due to the thicker Si absorber but also due to an increased absorption over the whole wavelength range of 750–1200 nm. As a result, a total current density of 38.8 mA/cm^2 is achieved, which is remarkably high considering the NIR loss in the 140-µm-thick Cz-Si-based bottom cell. A tandem cell $V_{oc} = 1.91$ V is as expected for this type of perovskite cell on the *thin* bottom cell, apparently, not performing less on the nano-texture as compared to flat wafer surfaces. The *FF* is about 1% (abs) lower than typically achieved *FF*s for our best tandem cells on FZ-Si.[20,23] This, however, might be ascribed to limited statistics in our case here. In total, the good performance of the tandem device gives indication of good perovskite coverage and no shunted areas in the active area. This is also indicated by SEM images as shown in Figure 7C. The cross-section image shows that the (small) pyramids are well covered by the perovskite layer, with thicknesses ranging between 400 and 750 nm, due to the non-planar substrate.

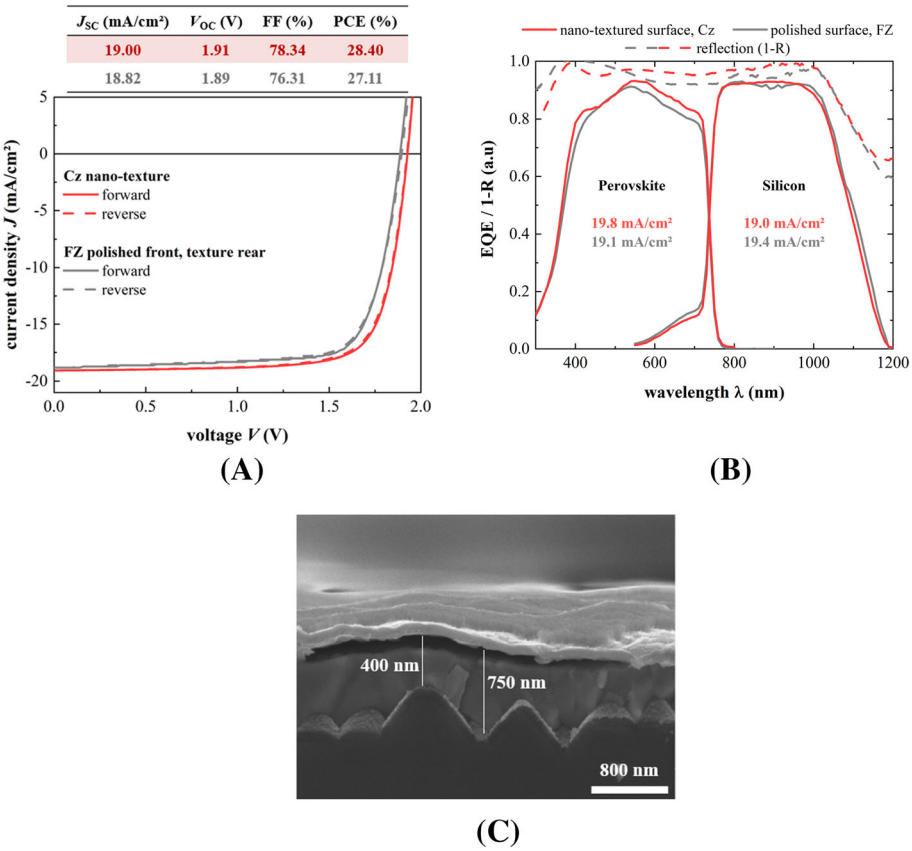


FIGURE 7 Perovskite/silicon tandem solar cell (A) *JV* data and (B) external quantum efficiency (EQE) measurement of the champion device; (C) scanning electron microscopy image of the cross-section of a tandem with a nano-textured bottom cell. *FF*, fill factor; PCE, power conversion efficiency.

4 | CONCLUSION

To summarize, we showed that anisotropic surface etching of random pyramids in the sub-micrometer range is an appealing process for industrial SHJ single junction solar cells and even more interesting for industrialization of high-efficiency monolithic perovskite/SHJ tandem solar cells. For tandem cells, a uniform and small-sized Si texture is crucial in order to be able to wet process the perovskite top cell. We showed that sub-micrometer sized random pyramids by an adjusted wet etching process are an interesting approach not only for such tandem solar cells but also for SHJ single junction solar cells. By finding an optimum composition of the etching solution, the pyramid height and distribution can be adjusted. We confirm the results previously shown in[4] that by adding K_2SiO_3 and increasing its volume fraction, the etching reaction is retarded, resulting in smaller pyramids. Strongly depending on the type of commercial additive, the pyramid height and density change significantly, leading to different electrical and optical performance of SHJ solar cells. The reflectivity of wafers can be kept similar and current losses in cells are completely avoided as compared to micrometer-sized standard textured Si. Excellent passivation quality was measured on nano-textured and passivated surfaces with lifetimes in excess of 5 ms, which we propose is due to lower a-Si:H/c-S surface recombination. All *JV* parameters were similar or even slightly better as compared to those of cells with our standard micro-texture.

Finally, we demonstrated the high potential of nano-textured SHJ cells in perovskite/silicon tandem solar cells, reaching an efficiency of 28.39% with a both sided nano-textured surface on Cz-Si-based bottom cell, compatible with industrial production. We successfully developed a textured surface with small pyramids and a narrow height distribution that is suitable to be covered completely with a solution-processed perovskite layer. We expect that the presented processes will be easy to be implemented in industrial production and, hence, will contribute to the development of a production process for highly efficient tandem solar cells.

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CONFLICT OF INTEREST

The authors declare no conflict of interest.

DATA AVAILABILITY STATEMENT

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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