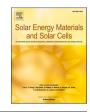


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Optoelectrical analysis of TCO+Silicon oxide double layers at the front and rear side of silicon heterojunction solar cells

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ARTICLE INFO

Keywords: Silicon heterojunction Thin transparent conductive oxide Optoelectrical analysis Bifacial IR reflector Power loss

ABSTRACT

Silicon Heterojunction has become a promising technology to substitute passivated emitter and rear contact (PERC) solar cells in pursuance of lower levelized cost of electricity through high efficiency devices. While high open circuit voltages and fill factors are reached, current loss related to the front and rear contacts, such as the transparent conductive oxide (TCO) layers is still a limiting factor to come closer to the efficiency limit of silicon based solar cells. Furthermore, reducing indium consumption for the TCO has become mandatory to push silicon heterojunction technology towards a terawatt scale production due to material scarcity and costs. To address these issues dielectric layers, such as silicon dioxide or nitride cappings are implemented to reduce TCO thicknesses both diminishing parasitic absorption and material consumption. However, reducing the TCO thickness comes in cost of resistive losses. Furthermore, the TCO properties do vary with thickness and neighboring layer configuration altering the optimization frame of the device. In this paper we present a detailed analysis to quantify the optoelectrical losses trade-off associated to the TCO thickness reduction in such layer stacks. Through the analysis we show and explain why experimental bifacial cells with 20 nm front and rear TCO perform at a similar level to reference cells with 75 nm under front and rear illumination reaching efficiency close to 24% at 92% bifaciality. We present as well a simple interconnection method via screen printing metallization to implement a thin TCO/silicon dioxide/silver reflector enhancing current density from 39.6 to 40.4 mA/cm² without compromising resistive losses resulting in a 0.2% absolute solar cell efficiency increase from a bifacial design (23.5–23.7%). Finally, following this approach we present a certified champion cell with an efficiency of 24.6%.

1. Introduction

Silicon Heterojunction (SHJ) solar cells are a major prospect to become a key technology for further deployment in mass production for the photovoltaics market. A very efficient wafer passivation allows open circuit voltages (V_{OC}) surpassing 750 mV and high fill-factors (FF) above 84% even on full wafer scale [1]. Record SHJ solar cells reach power conversion efficiencies (PCE) of 26.7% for an interdigitated back contacted (IBC) lab cell [2] and above 25% for two-side contacted solar cells [3–6]. Low processing temperatures <200 °C and the symmetric device stack facilitate thin wafers and high bifaciality (front to rear

illumination PCE ratio) of cells, both favorable for low levelized cost of electricity (LCOE). One limitation to further approach the efficiency limit of silicon solar cells is the insufficient lateral conductance of the wafer thin-film silicon layer systems adding the requirement of transparent conductive oxide (TCO) layers to achieve a low resistive carrier transport to the metal electrodes. The TCO is constrained to thicknesses of 60–80 nm to act simultaneously as an anti-reflective coating (ARC) [7, 8]. This results, however, in parasitic absorption losses of approx. 0.8 mA/cm² at the front and 0.3 mA/cm² at the rear side of the device [9]. One possibility to decrease these losses is reducing the TCO thickness (t_{TCO}) with a further benefit of diminishing material consumption. This

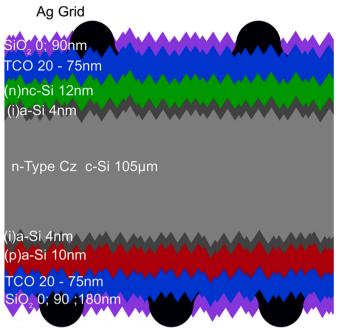
https://doi.org/10.1016/j.solmat.2021.111493

Received 19 May 2021; Received in revised form 8 November 2021; Accepted 8 November 2021 Available online 1 December 2021 0927-0248/© 2021 The Authors. Published by Elsevier B.V. This is an open access article under the CC BY license (http://creativecommons.org/licenses/by/4.0/).

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Ag Grid or Ag Rear Reflector

Fig. 1. Bifacial rear-junction Silicon Heterojunction standard solar cell structure as used for simulations and experiments in this study.

has become essential for the perspective of a future terawatt scale mass production due to the scarcity of Indium which is contained in typical TCO industrial applications [10].

To open the possibility of reducing $t_{\rm TCO}$, a dielectric layer such as silicon dioxide (SiO₂) or silicon nitride (a-SiN_x) can be implemented on top of the TCO obtaining 0.4–0.8 mA/cm² current generation ($J_{\rm Gen}$) enhancement by reducing front reflectance and parasitic absorption in the TCO [9,11–13]. However, reducing $t_{\rm TCO}$ compromises resistive losses, requiring a careful analysis for device optimization.

In this work, we perform 2-dim optoelectrical simulations of bifacial SHJ solar cells electron and hole selective contacts considering $t_{\rm TCO}$ and, TCO carrier concentration ($n_{\rm e}$) variations for optimized grid finger pitch and SiO₂ capping layers. We emphasize the importance of separating the analysis of the electron (front illumination) and the hole (rear illumination) selective contacts to gain insight in the expected behavior of bifacial solar cells, considering that the transport losses differ for each contact [9,14–16]. The simulations show the optimization paths for $t_{\rm TCO}$ reduction from 80 to 20 nm by quantifying the optoelectrical trade-off involved. Experimental devices are manufactured to confirm the trends. It is observed that solar cells with very thin front and rear 20 nm $t_{\rm TCO}$ can achieve PCE close to 24%, similar to reference cells with standard 75 nm TCO thickness.

To further benefit from the 20-nm thin rear TCO, we also present a monofacial contacting scheme with a screen-printed grid on top of the thin rear TCO that is subsequently coated with a 180 nm SiO₂ and a sputtered silver (Ag) reflector. This enables the interconnection of the TCO to the Ag reflector through the SiO₂, without increasing R_S losses and increasing generated current density J_{Gen} from 39.6 to 40.4 mA/cm² resulting in a 0.2% PCE increase. Such a reflector can be implemented for thin Silicon (Si) wafers as well as bottom solar cells for tandem applications for which the IR response increases its relevance. Finally, by combining such a reflector with a further improved TCO a certified efficiency as high as 24.6% is reached.

2. Experimental methods

2.1. Solar cells preparation and characterization

Solar cells were prepared using n-type Czochralski (CZ) silicon wafers (c-Si) with 5 Ωcm resistivity. The as-cut wafers were wet-chemically etched to eliminate the sawing damage. Its surfaces were then textured in KOH to obtain random pyramids with heights in the range of 1–3 µm with <111> oriented facets and resulting in ${\sim}105~\mu m$ thick wafers. After RCA cleaning and a dip in a 1% diluted hydrofluoric acid solution, nominally 4 nm (i)a-Si:H plus 10 nm (p)a-Si:H layers were deposited at the rear side of the wafer to form the hole contact (rear junction). For the electron contact at the front side a 4 nm (i)a-Si:H and 12 nm nanocrystalline (n)nc-Si:H stack was deposited. The depositions were carried out by plasma-enhanced chemical vapor deposition (PECVD) in an AKT1600 cluster tool from Applied Materials with a parallel electrode configuration operated at 13.56 MHz. Indiumoxide based TCO layers were sputtered through aligned shadow masks on both sides of the wafer to define 12 4-cm² sized cells and two transfer length method (TLM) structures per wafer. For further details on the TCO deposition, please refer to the next subsection. A silver grid with a 1.7 and 0.8 mm fingerpitch was screen printed at the electron and hole contact of the solar cells, respectively.

The grid was cured at 210 °C for 20 min on a hot-plate under atmospheric conditions. On top of the front and rear finished contacts a 90 or 110 nm PECVD SiO₂ layer was deposited. For the monofacial devices the rear SiO₂ had 180 nm thickness and a 400 nm sputtered Ag reflector. All cells were heat-light-soaked under 1 sun for 5–10 min on a hot-plate at 210 °C. Fig. 1 shows the schematic cross section of the described bifacial SHJ solar cell. The solar cells were characterized using current density voltage (*J*–*V*) measurements in the dark and under a calibrated AM1.5G spectrum on a NIR reflective chuck. Resistance measurements were performed on the TLM structures to calculate the TCO sheet resistance (R_{Sh}) on devices. R_S values of the solar cells were determined from the dark to light *J*–*V* curve comparison according to Ref. [24].

2.2. TCO layer stacks preparation and characterization

To investigate the TCO film properties on different substrates, 1.1 mm thick Corning Eagle XG glasses were used. Intrinsic and doped silicon layers as described above for the solar cells were deposited on some of the samples. On top of these coated substrates as well as on bare glass TCO layers with 28 and 110 nm nominal thickness were deposited in an in-line DC magnetron sputtering system from Leybold Optics (A600V7). The indiumoxide-based TCO layers were sputtered from a rotatable target (600 mm, type "newSCOT" from ANP corp.) without intentional heating with oxygen flow ratios relative to Argon (Ar) of 0.8, 1.8, 2.2 and 3.2% for the layers with 4.1, 2.0, 1.5 and 0.6 \times 10²⁰ cm⁻³ carrier concentration, respectively. All depositions were carried out under 0.5% hydrogen (H₂) flow relative to Ar. For characterization, the samples were annealed on a hot-plate at a temperature of 210 °C for 15 min in ambient atmosphere. Charge carrier mobility μ_e , and concentration, n_e , were determined for TCO layers on glass by Hall measurements with an Ecopia HMS 3000 system applying the van der Pauw geometry at room temperature. Refractive indices n and extinction coefficients k of the TCO samples deposited on glass and on flat silicon substrates were extracted from spectrophotometer and spectroscopic ellipsometry measurements by fitting to a Drude-Tauc-Lorentz model for optical simulations [17].

3. Results and discussion

3.1. Simulations: optical vs resistive losses

Since the implementation of a second ARC, in this case SiO₂, opens the flexibility to reduce the TCO thickness, understanding the behavior

Table 1

Parameter variations used for optical (GenPro4 [18]) and electrical (Quokka3 [19]) simulations.

TCO Thickness [nm]	20-80 20 units steps
TCO $\mu_{\rm e}$ [cm ² /Vs]]	35-45
TCO $n_{\rm e} [{\rm x10^{20} cm^{-3}}] (R_{\rm SH})$ @75 nm[Ω])	0.6 (500), 1.5 (195), 2.0 (130), 4.1 (80)
Grid Finger Pitch [mm]	0.8, 1, 1.5, 2, 2.5
TCO-Si contact resistivity	Electron Contact: 50
$\rho_{\rm C} \ [m\Omega cm]$	Hole Contact: 150
Reference J _{SC} [mA/cm ²]	Electron Contact Illumination (Front): 38.5
@AM1.5	Hole Contact Illumination (Rear): 36.7
Wafer properties	CZ mono n-type; $t = 105 \ \mu\text{m}; \rho = 5\Omega\text{cm};$ mid-gap SRH
	$\tau_{\rm n} = 1000 \mu { m s}, \ au_{ m p} = 10\ 000 \mu { m s}; \ { m both-side \ textured} \ [20]$
Grid Finger Properties	$w = 40 \ \mu\text{m}; h = 15 \ \mu\text{m}; \rho_{\text{line}} = 1.6 \ \Omega/\text{cm}; R_{\text{Sh}} = 65\Omega; \rho_{\text{C}}$
	$= 0.5 \text{ m}\Omega\text{cm}$
Unit Cell Geometry	$x = 1000 \ \mu m \ y = 2000 \ \mu m$ (x-Finger y-Busbar
	direction)

of the optical and electrical power losses ($P_{\rm Loss}$) trade-off in this scenario becomes important. In this section, we present an optoelectrical analysis of SHJ solar cells by varying TCO thickness and TCO $n_{\rm e}$, for an optimized grid-finger pitch (0.8–2.5 mm). We address the optimization of the hole and electron contact for standardized AM1.5 illumination conditions in air. Throughout the manuscript the electron contact illumination case is referred to as front whereas the hole contact illumination is referred to as rear. An extension of the analysis for the application in bifacial modules should consider different front-side as well as rear-side illumination conditions depending on geographical location, system orientation, meteorological year, albedo amongst others as well as different cell interconnection methods, which is out of the scope of this paper.

The varied and main parameters utilized as input for optical (Gen-Pro4 [18]) and electrical (Quokka3 [19]) simulations are presented in Table 1.

Fig. 2a) and b) show the results of the solar cell optical and carrier transport P_{Loss} for the electron and the hole contact, respectively. For each contact, the maximum J_{SC} of 38.5 and 36.7 mA/cm² for front and rear, respectively, are considered as reference values for optical losses. Note that the rear reference J_{SC} is 1.8 mA/cm² lower than the front due to the optimization of the thin-film silicon layers for front illumination. The resistive P_{Loss} shown in Fig. 2a) for front illumination account only for the electron transport whereas for rear illumination in Fig. 2b) only for the hole transport. These include lateral, vertical, and grid finger transport losses for the respective charge carrier type. Separating the P_{Loss} of the electron and hole selective contacts allows for the optimization of both sides aiming for highest bifaciality. For the discussion of

the results, please note that the different TCOs will be referred to with their carrier concentrations (0.6, 1.5, 2.0 and 4.1). From the results in Fig. 2a) we can observe that the 4.1 TCO is not competitive with lower doped TCOs due to very high optical loss. The lowest P_{LOSS} for this TCO found at 20 nm is 1.26 mW/cm² compared to 0.92, 0.76, 0.80 mW/cm² for the 0.6, 1.5 and 2.0 TCOs, respectively. The optima are found at 40-60 nm thickness for the lower doped TCOs, 20 nm being too resistive and 80 nm presenting high optical loss. A similar behavior is observed for the hole contact. In this case, however, the electrical transport losses are inherently higher due to a lower hole mobility and the higher contact resistance of the TCO/(p)a-Si:H/(n)c-Si in comparison to the TCO/(n)a-Si:H/(n)c-Si [16,21-23]. Hence, for all optimized stacks the hole contact presents higher P_{Loss} compared to the electron contact. The lowest P_{Loss} systems at $n_{\rm e} = 1.5 {\rm e2 cm}^{-3}$ and 60 nm for both contacts present 0.76 and 0.83 mW/cm^2 for the electron and hole contact, respectively. This is explained by the resistive losses differences. For this reason, a bifacial solar cell should be positioned in the module with the electron contact facing the highest irradiated side. Analyzing now the possibility of reducing TCO thickness to 20 nm, the optima are found at $n_e =$ 2e20cm⁻³ for both electron and hole contacts with 1.03 and 1.31 mW/cm² P_{Loss} , respectively. This is 0.21 and 0.41 mW/cm² higher P_{Loss} than the 80 nm reference thickness for the electron and hole contact as well as 0.31 and 0.48 mW/cm² respectively to the overall optima. Hence, thinning the TCO to 20 nm comes in cost of around 0.3% absolute efficiency for front and 0.5% for rear illumination, respectively.

An additional aspect that must be considered is the effect of the contact resistivity ($\rho_{\rm C}$). As several authors have investigated the TCO to Si $\rho_{\rm C}$ varies in dependence of TCO $n_{\rm e}$ decreasing with increased values [23–27]. In our simulations, however, $\rho_{\rm C}$ is kept constant as measured through transfer length method (TLM) [28] structures for the reference electron contact ($n_e = 2.0e20cm^{-3}$) and via an R_s breakdown [16,22] for the hole contact ($n_e = 1.5e20cm^{-3}$). Hence, it is expected that the $n_e =$ 4.1 TCO resistive P_{Loss} are overestimated and oppositely the 0.6 TCO underestimated. This discards the application of the low doped 0.6 TCO, since it shows already higher P_{Loss} than the 1.5 and 2 TCO at equal ρ_{C} . The 4.1 TCO can be discarded as well, since even with a $\rho_{\rm C} = 0\Omega {\rm cm}$ its P_{Loss} is higher than the one for $n_{\text{e}} = 2$ due to the high optical loss in this case. For the investigated TCO with $\mu_e = 40-45 \text{ cm}^2/\text{V}$, it is concluded that a good balance minimizing $P_{\rm Loss}$, is found for middle-range TCOs with $n_{\rm e}$ between 1.5 to 2×10^{20} cm⁻³ since the highly doped TCO increases optical losses that cannot be counterbalanced by a resistive losses decrease. A low doped TCO $n_{\rm e} = 0.6 \times 10^{20} {\rm cm}^{-3}$ will show the opposite effect. An increased TCO μ_e would shift the optima to lower n_e values, assuming constant contact resistivity.

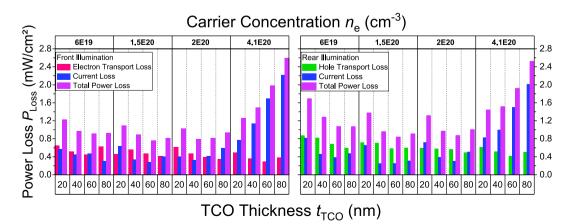


Fig. 2. a) Simulated current density (J_{SC}) and electron transport power losses (P_{Loss}) with respect to the reference cases for an electron contact illuminated silicon heterojunction solar cell. TCO carrier concentration (n_e) and TCO thickness (t_{TCO}) are varied for optimized grid finger pitch between 0.8 and 2.5 mm. b) Same as a) but for hole transport power loss and hole contact illumination (rear-side).

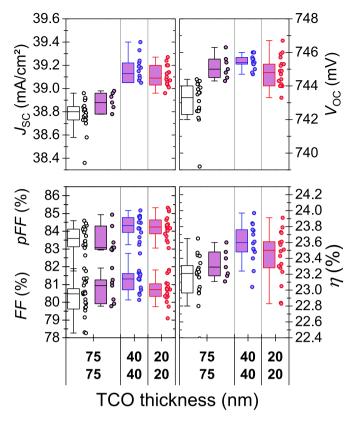


Fig. 3. *I*–V Parameters of solar cells with varied electron contact (Front) and hole contact (Rear) TCO thickness. The reference 75 nm front and rear TCO cells are shown in black and no-fill boxplots. The boxplots with violet fill represent solar cells with 90 nm SiO_2 deposited on both front and rear TCO. Blue and red boxplots are for 40 nm front and rear TCO and 20 nm front and rear TCO, respectively. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

3.2. Experimental solar cells: TCO thickness variation

To verify the theoretical results experimental solar cells were processed. Fig. 3 shows J-V parameter results of the solar cells before and after a 90 nm SiO₂ deposition on both sides of the solar cells. The first group are reference devices with standard front and rear 75 nm TCO thickness which are presented before and after SiO₂ whereas the next groups became thinner TCO layers of 40 nm front and rear as well as 20 nm front and rear thickness. From this point the groups will be referred to as 75, 40 and 20.

After SiO₂ deposition we observe a J_{SC} increase for the 75 cells expected from ARC improvement [9,11,13]. The groups with thinner TCO present a slight increase in J_{SC} compared to the reference device due to lower parasitic absorption in the TCOs. Comparing before and after SiO₂ deposition, the $V_{\rm OC}$ of the 75 solar cells slightly increases, however, this is a marginal increase and all cells for all groups present V_{OC} between 742 and 746 mV. After SiO₂ deposition a slight R_S reduction is observed in all cases as it is exemplified by the 75 devices in the pseudo fill-factor (pFF) minus FF change. Furthermore, the 40 and 20 cells groups show very similar *pFF-FF* compared to the 75 cells meaning that the resistive losses of the cells with thinner TCOs do not present a strongly detrimental effect. Finally, we observe that all groups show similar median efficiencies of 23.3, 23.6 and 23.5% for the 75, 40 and 20 cells respectively with a best cell for the 40 group with 24% followed by a 23.9% cell in the 20 group. Furthermore, all cells show a bifaciality of 90–93% which has been shown to be an optimal value for a 20-40% back-side irradiance relative to the front [29,30]. These results show that SHJ solar cells with up to one fourth of the thickness of the standard TCO can be produced without any efficiency penalty.

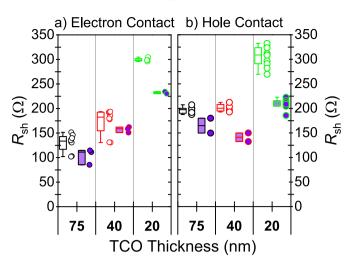


Fig. 4. Transfer length method (TLM) measurements with different TCO thicknesses on a) the electron contact with (n)nc-Si:H thin film silicon and b) the hole contact with (p)a-Si:H thin film silicon. The boxplots with violet fill represent the values of TLM structures after 90 nm SiO_2 deposition. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

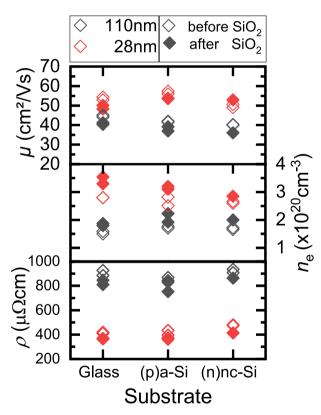


Fig. 5. Hall measurements, mobility μ_{e} carrier concentration n_{e} and resistivity ρ of TCO on different glass and coated substrates before (empty symbols) and after a 90 nm SiO₂ (filled symbols) deposition.

To gain further insight into the behavior of a reduced R_S and the TCOs properties after SiO₂ deposition we analyzed TLM structures on the same wafer as the cells that show the sheet resistance $R_{\rm Sh}$ behavior of the TCO layers.

Fig. 4 shows two interesting effects for both TCO layers deposited at

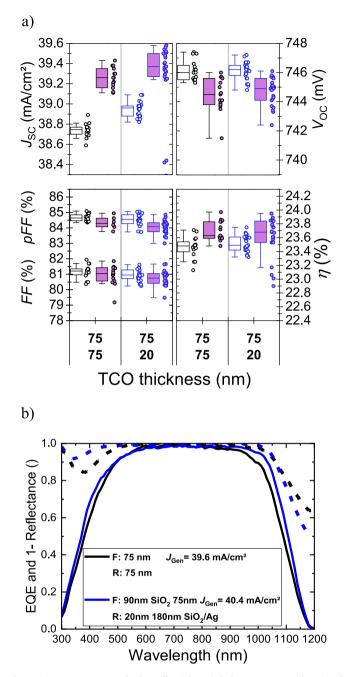


Fig. 6. a) *I–V* Parameters of solar cells with varied electron contact (front) and hole contact (rear) TCO thickness before (empty boxplots) and after a front 90 nm and rear 180 nm SiO₂ plus silver reflector deposition (violet filled boxplots). *I–V* measurements were done on a NIR reflective chuck. b) EQE and 1-reflectance measurements for the reference bifacial solar cells (black empty boxplot in a)) compared to solar cells with 75 nm front and 20 nm rear TCO plus 90 nm front 180 nm rear SiO₂ plus Ag (violet filled blue boxplot in a)). EQE measurements were done w/o reflective chuck and w/o accounting for front-grid losses. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

the front electron contact (left) and at the rear hole contact (right). We observe that the $R_{\rm Sh}$ of all TCO layers is reduced after SiO₂ deposition. This is especially clear for the 20 nm layers which reduce their $R_{\rm Sh}$ from 300 to 225 Ω (electron contact). Furthermore, we observe an unexpected

behavior in which the almost four times thinner 20 nm TCO layer increases its R_{Sh} only by a factor 2.3 on the electron contact and by a factor of 1.6 on the hole contact, as compared to their 75-nm counterparts. In order to elucidate these findings, we analyzed witness glasses, namely, without coating, with an i/p amorphous silicon layer stack and with an i/n nc-Si layer stack co-deposited with the analyzed TLM structures and solar cells. Please note, that the priorly described layer thicknesses were deposited on textured wafers and these are on a flat substrate. This explains the increased thicknesses from 20 to 28 nm and 75-110 nm. For the electron-contact type TCO samples shown in Fig. 5, we observe that the 28-nm thick layers show a higher μ_e on all substrate types well exemplified by the comparison on (p)a-Si:H were μ_e increases from 40 to 55 cm²/V. We see as well that all TCO layers show a lower μ_{ρ} on the nc-Si substrates. We observed this effect previously for ITO [31]. Also other authors have pointed out the influence of substrate layers on the growth of indium oxide based TCOs [32-35]. Furthermore, with decreased layer thickness, the $n_{\rm e}$ increases from 1.5 to around 2.5 \times 10²⁰ cm⁻³. The combined effect of increased μ_e and n_e leads to a resistivity decrease with lower TCO thickness from 900 to 400 μΩcm.

The clear differences between TCOs with varied thickness indicate the presence of graded TCO layers. The higher carrier concentration in the thinner TCOs is an explanation for the low series resistance increase when reducing TCO thickness in the experimental solar cells groups. Such thin higher doped TCO layers also open flexibility to tune the TCO carrier concentration aiming for decreased contact resistance, as it was shown by Leilaeioun et al. and Luderer et al. and without strongly compromising optical performance [23,27].

3.3. Monofacial case with a SiO₂/Ag reflector

A possibility to enhance the solar cell efficiency is to add an Ag reflector on top of the 20 nm TCO plus SiO₂ layer stack on the rear side. For this purpose a thicker SiO₂ layer of around 180 nm has to be introduced in combination with the thin TCO in order to avoid evanescent plasmonic absorption in the Ag as was described by Holman et al. [36]. In fact, Holman et al. used a masking mesh on top of the TCO during MgF deposition to maintain free open areas for the metal contacting. This approach resulted in an SHJ solar cell efficiency benefit from 20.7 to 21.2% [12]. More recently, Boccard et al. reported that this contacting scheme can successfully increase J_{SC} by 0.6 mA/cm² but they encountered FF and V_{OC} losses when processing this approach for solar cells with efficiency >24% [37]. Here, we show a simple alternative contacting scheme with a standard screen-printed Ag grid on top of the 20-nm thin TCO that is subsequently capped with a 180-nm thick SiO₂ by PECVD. The 400-nm thick Ag reflector sputtered on top makes good contact to the silver grid lines w/o electrical loss even through the SiO₂ capping.

Such a monofacial contacting scheme enables the introduction of the J_{SC} improving SiO₂ layer w/o additional R_S losses compared to the actual bifacial solar cell. Such a reflector however is probably more useful to boost cell's efficiency in the lab. For commercial production, usually preferring the bifacial cell design, the two additional process steps come with extra costs.

We processed monofacial solar cells to investigate the behavior of such a reflector on high-efficiency devices. Fig. 6 shows the results for solar cells with 75 nm front and rear TCO compared to 75 nm front and 20 nm rear TCO. On the left in bifacial design and on the right after 90 nm front SiO₂ deposition and 180 nm rear SiO₂ plus 400 nm Ag deposition.

After adding the enhanced back reflector, the J_{SC} of the reference cell increased by 0.5 mA/cm², as determined from J-V measurements on our NIR-reflective chuck.

Decreasing the rear TCO thickness to 20 nm slightly further increases J_{SC} by 0.1 to 39.4 mA/cm². The enhancement results in 0.2% absolute efficiency increase from the standard bifacial device. The thin TCO layer can be further optimized according to the resulting adapted 20 nm TCO

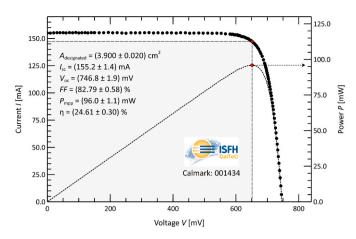


Fig. 7. I–V curve and parameters of champion SHJ solar cell measured at ISFH-CalTeC.

properties presented in Fig. 4. External quantum efficiency measurements (EQE, w/o front grid and w/o NIR-reflective chuck) with the reference bifacial layer stack compared to the enhanced reflector confirm the improved infrared spectral response as well as the ARC effect at the front resulting in 0.8 mA/cm² J_{SC} increase.

3.4. 24.6% champion cell

With the above described approach and a further improved TCO process we reached a cell efficiency of 24.61%, certified by ISFH as observed in Fig. 7. On the front a 110 nm SiO₂ layer is applied as ARC on top of a 75 nm thick TCO and the screen-printed grid. On the rear side a 20 nm thick TCO was deposited subsequently followed by a screen-printed grid and a SiO₂/Ag reflector. Due to the increased charge carrier density in such thin films a low TCO/(p)a-Si:H/(n)c-Si contact resistance could be maintained. Additionally, the alternative contacting scheme allowed a good contact through the SiO₂ layers leading to a series resistance of 0.55 Ω cm² (in-house measurement). To reduce the parasitic absorption the TCO deposition parameters were further adapted leading to a J_{SC} of 39.8 mA/cm². According to the findings described in this paper a thinner front TCO will improve the J_{SC} even more without suffering from electrical losses.

4. Summary and conclusions

We presented simulations to quantify optoelectrical losses of SHJ solar cells with SiO₂/TCO layer stacks in dependence of TCO thickness and carrier concentration. For an optimized grid and for a TCO with mobility around 40 cm²/V, a highly doped TCO with 4.1 × 10²⁰cm⁻³ carrier concentration comes with high optical power losses whereas a 0.6×10^{20} cm⁻³ lower doped TCO comes with high resistive losses. An optoelectrical balance for an optimal TCO design is found in the midrange carrier concentration at $n_e = 1.5-2.0 \times 10^{20}$ cm⁻³. Comparing the electron contact to the hole contact, for all optimized stacks the hole contact presents higher P_{Loss} , hence bifacial SHJ solar cells should always be positioned with the electron contact facing the highest irradiated side in a module.

We demonstrate with experimental results that SHJ solar cells with 20 nm front and rear TCO thickness plus SiO_2 capping layers can perform similarly to standard thickness TCO cells of 75 nm. This allows a 75% TCO material reduction reaching 23.9% efficiency.

Finally, we present an enhanced rear reflector with a 20 nm thin TCO, an Ag screen printed grid, 180 nm SiO₂ and a full-area silver reflector, in combination with front ARC, that enhances current density by 0.8 mA/cm² showing a 0.2% absolute efficiency increase from a bifacial solar cell. Through the applied optimization approaches a

certified solar cell efficiency of 24.61% is reached.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Acknowledgment

We would like to thank the co-workers at HZB for their support.

Katja Mayer-Stillrich and Manuel Hartig for sputtering depositions. Mathias Zelt and Tobias Henschel for support with PECVD. Jannik Niels Kleesiek for screen-printing processing. Franziska Biegalke, Denise Debrasine and Maxim Simmonds for device characterization. This work was partially supported by the German Ministry of Economic Affairs and Energy, Germany (BMWi) in the framework of the Dynasto (0324293B) and ProSelect (0324189C) projects.

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