Solid Electrolyte Interphase Layer Formation during Lithiation of Single Crystal Silicon Electrodes with a Protective Aluminum Oxide Coating

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Abstract

The lithiation of crystalline silicon was studied over several cycles using *operando* neutron reflectometry over 6 cycles. A thin layer of aluminum oxide was employed as an artificial coating on the silicon to suppress the SEI-layer related aging effects. Initially the artificial SEI prevented side-effects, but lead to an increased lithium trapping. This layer degraded after two cycles, followed by side reactions, which decrease the coulombic efficiency. No hint for electrode fracturization was found even though the lithiation depth exceeded 1 μ m. Two distinct zones with high and low lithium concentration were found, initially separated by a sharp interface which broadens with cycling. The correlation of the reflectometry-results with the electrochemical current showed the lithium fraction that is lithiated in the silicon and the lithium that remained inside of the silicon. Additional electrochemical impedance spectroscopy was used to gain insights into the electrical properties of the sample via fitting to an equivalent circuit.

Introduction

Silicon is considered as potential electrode material for next-generation lithium-ion batteries (LIB) due to their high specific capacity of up to 4200 mAh/g ^{1–3}. This storage ability is approximately one order of magnitude higher than current graphite electrodes ². Moreover, silicon does not harm the environment and is non-toxic ³. It is widely used in industrial processes and Si is abundant ^{1,2}. However, the successful commercialization of silicon electrodes faces several challenges. The high specific capacity is accompanied by a volume expansion of up to 310% during lithium uptake ^{1,2}. This deformation causes mechanical degradation of the electrode and continuous consumption of electrochemically active material for SEI-layer growth ². Therefore silicon electrodes experience a fast capacity decay during cycling, which limits their applications ^{1–3}. One potential way to overcome these shortages is the use of artificial coatings ^{4–10}. A thin layer

on top of the silicon electrode can prevent direct contact of electrolyte and electrode and, therefore, suppress the SEI-layer formation ⁵. Furthermore, mechanical confinement decreases the electrode's mechanical stress, leading to a decreased fracturization ⁵. Different materials as artificial coating have been studied, such as LIPON ^{6,11,12}, titanium oxide ^{13,14}, or aluminum oxide/alucone ^{7,15–18}. LIPON-coatings require thicknesses larger than 50 nm to work effectively as a protective coating, limiting its high-rate capabilities and improving mechanical properties ^{6,12}. Jin *et al.* and Yu *et al.* studied titanium (sub)-oxide-coated nanoparticles, showing the silicon's effective confinement within the protective coating ^{13,14}. In their theoretical study, Jung *et al.* investigated lithium transportation through an aluminum oxide layer on silicon electrodes ¹⁵. They found increased lithium mobility for lithiated aluminum oxide. He *et al.* studied the use of alucone using *in-situ* TEM ⁷. They present improved electronic properties of the silicon particles due to the absence of lithium oxide. Hy *et al.* and Becker *et al.* showed the decreased SEI-layer growth on



Figure 1: Scheme of the *operando* experiment. On the left, the employed *operando* cell is shown. A sketch of the probed region is illustrated in the middle. The right panel shows the evolution of the sample during the course of the experiment.

aluminum oxide coated silicon electrodes in combination with electrolyte additives ^{16,17}. DeCaluwe *et al.* employed *in-situ* neutron reflectometry to study an aluminum oxide coated silicon electrode ¹⁸. In their study, no conventional SEI-layer formed from decomposition products of the electrolyte. Furthermore, the growth and shrinkage of pores within the silicon electrode was proposed. However, a detailed analysis of the lithiation mechanism through the protective layer is still missing. *Operando*-studies may help to get a holistic view of the influence of an artificial SEI-layer. Here we present an *operando* neutron reflectometry study of the lithiation mechanism of a single-crystal silicon electrode coated with aluminum oxide. A scheme of the experiment is shown in fig. 1. Single crystalline silicon electrodes serve as a model system since they work without binders or conductive agents. This approach allows us to gain fundamental insights into the lithiation process of silicon and correlate this to morphological observations. The high contrast of silicon and lithium qualifies neutron techniques as an ideal tool to investigate the lithiation process ¹⁹. Neutron reflectometry (NR) is the method of choice due to the high sensitivity of reflectometry towards thin layers in the nm-range ^{20,21}. Additional electrochemical impedance spectroscopy (EIS) links the observed structural evolution to the electrochemical properties of the system.

This paper is organized as follows: First, the pre-characterization of the electrode will be shown, followed by a discussion of the electrochemical data and EIS-results. Afterward, the connection with the structural data obtained by *operando*-NR will lead to a holistic view of the lithiation process.

Results and Discussion

Pre-characterization of the system.

A 3 nm layer of aluminum was deposited on the silicon wafer using electron beam evaporation without removing the native silicon oxide layer. The sample was stored in the air afterward to allow the formation of the aluminum oxide layer. Before the neutron experiments, the coated Sielectrode was characterized using X-ray reflectometry (XRR). With this technique, it is possible to probe a large portion of the samples surface, similar to neutron reflectometry, without destroying the sample. The obtained data, together with the fit and the resulting scattering length density (SLD)-profile are shown in fig. 2. The SLD is the product of two material properties, namely the atomic scattering length and number density ²². It influences the refractive index of the material for the incoming radiation (in this case X-rays or neutrons) and leads to reflections according to the Fresnel laws ²⁰. For comparison, the NR curve and SLD profile of the silicon's virgin state of are added in the same figure.



Figure 2: Pre-characterization of the sample. The scattering curves are shown on the left together with the fit. The resulting SLD-profiles are shown on the right. The dashed lines denote the individual layers.

There are two additional layers on top of the silicon wafer (XRR-results). The outer layer is the aluminum oxide layer, whereas the inner layer is ascribed to the native silicon oxide layer 23,24 . Within the native silicon oxide layer, a minimum of the SLD-value of approx. 16 x 10⁻⁴/nm² can be observed, which indicates a varying mass density within the film. The interplay of both layers, the native oxide and the aluminum oxide layer, leads to the dip in the X-ray SLD-profile at 3 nm, since both layers exhibit a high roughness compared to the layer thickness. The outer layer has a thickness of approximately 6.5 nm and exhibits a high roughness towards the air. This indicates the presence of voids and pores since the thickness of the coating is higher than the expected value. The resulting SLD-value is a mixture of aluminum oxide coating in their study, but roughly half of the expected value. The total amount of aluminum oxide within the layer corresponds to a 3.3 nm thick aluminum oxide layer (assuming Al₂O₃) without pores. This result is close to the deposited amount of 3 nm of aluminum. Therefore, it is unlikely that the inner layer contains metallic aluminum. It is more likely that a native silicon oxide layer with a thickness of 1.8 nm is underneath this porous aluminum layer. This thickness was also observed previously ^{7,22,25}.

Electrochemical results of the operando experiment

The electrochemical results of the *operando* neutron experiment are summarized in fig. 3. Part A shows the voltage and part B the applied current. Part C is the relative residuum of the fit to the EIS data, whereas part D shows the results of the fit, which are the cell resistance R_{sol} and the charge transfer resistances R_{ct} , which are split into a fast ($\tau < 1.5$ s) and a slow ($\tau > 1.5$ s) regime. The cell was left in open-circuit-voltage (OCV) mode for 13 h at the beginning to allow the wetting

of the electrode ^{26,27}. Electrochemical impedance spectroscopy (EIS) was performed at the beginning and the end of the OCV-period. The employed equivalent circuit used to model the data is shown in fig S2. The results show a cell resistance of 1.7 and 1.9 Ω (38.3 and 43.5 Ω ·cm²) before and after the wetting, respectively, which is higher than the values obtained on the uncoated silicon electrode ²⁸. Based on the ionic conductivity of the electrolyte given by Berhaut *et al.* ²⁹, a resistance of 0.8 Ω can be attributed tot he electrolyte, whereas the remaining part arises from the electrodes itself, the contact resistances etc.. DeCaluwe *et al.* observed a cell resistance of 29.7 Ω (~1021.7 Ω ·cm²), indicating increased cell resistance due to the aluminum oxide layer. In addition to cell resistance, two significant charge transfer processes can be found. The corresponding charge transfer resistances R_{CT} are equal to 15 Ω and 355 K Ω for the fast and slow processes. This difference indicates the presence of a charge-transfer inhibition, which takes place primarily at low frequencies. Such a charge-transfer inhibition can be caused by an initial SEI-layer found by Veith *et al.* and Seidlhofer *et al.* for uncoated silicon ^{22,30}. However, DeCaluwe *et al.* did not observe an additional SEI-layer on their coated Si electrode ¹⁸.

The cell was cycled afterward with a current of 250 µA for two cycles. In the first two cycles, no side reactions were detected from the voltage curve, which would be represented by a voltage plateau above the lithiation voltage during discharge. The lithiation of amorphous silicon can be observed in the second cycle, which is frequently described in the literature ^{1,2,22,25,31}. In total, the lithiation for the first and second cycle took 3 and 3.2 h, respectively. The final cell voltage at the end of the lithiation was slightly negative (-4 and -20 mV). These values indicate an overpotential caused by the protective coating and the additional associated resistance ¹⁵. The delithiation took 2.5 and 2.6 h for the first and second cycle, leading to a Coulombic efficiency of 83 and 81 %, respectively. This low charge retention indicates either side reactions, a leakage current, or lithium trapping in the silicon, as reported by Jerliu et al. and Rehnlund et al. ^{32,33}. However, an increase in the Coulombic efficiency compared to the uncoated cell would be expected, as described by Ai et al. ³⁴. The current was increased within the third cycle since a long voltage plateau was observed around 550 mV. This observation indicates ongoing side reactions ³⁵, which should be suppressed by the aluminum oxide coating ⁴. Ha et al. proved traces of humidity within the electrolyte may lead to side reactions at these voltages, including the formation of HF³⁶. Once the current was increased, the voltage plateau dropped to lower voltage values and ended after roughly 5 h.



Figure 3: Electrochemical results of the *operando*-experiment. **Part A:** Voltage profile of the cell. OCV-periods are drawn in black. The galvanostatic cycling is shown in red and EIS-measurements are indicated with green Points. **Part B:** Cell current. Negative currents correspond to lithiation, whereas positive currents correspond to delithiation. **Part C:** Solution resistance (black) and charge transfer resistances obtained from the EIS-data. The charge transfer resistances are split into a fast (τ < 1.5 s) and slow (τ > 1.5 s) regime. The dashed lines indicate the beginning of a cycle.

From this point onwards, no negative voltages were observed during the lithiation. The subsequent cycles exhibit two additional plateaus between 1.5 V and 0.7 V, indicating further side reactions ^{37,38}. In all cycles, the delithation takes between 2.2 and 2.6 h, which is shorter than the

lithiation period (3 h). This indicates side reactions, a leakage current, or lithium trapping within the silicon.

The fast and slow charge transfer resistances that were obtained from the EIS show an alternating behavior. Both resistances decrease in the lithiation state, whereas they increase in the delithiated state by approximately one and 2.5 orders of magnitude for the fast and slow processes, respectively. From the third lithiation on, the R_{CT} values of the slow processes are roughly by a factor of four lower than for the first two cycles, meaning the charge transfer is enhanced at higher cycle numbers in the lithiated state. R_{ct, fast} also shows a different behavior, where the value in the lithiated state is decreased and in the delithiated state increased, each approximately by one oder of magnitude.

Of particular interest is the EIS performed before increasing the current in the third cycle. Here, a slight drop in the slow R_{CT} can be found, indicating an inhibition layer's decomposition. The cell resistance also shows small oscillations with the cell's charging state, which originate from the silicon's conductivity change during lithium insertion ³⁹. DeCaluwe *et al.* also observed this behavior ¹⁸. After six cycles, a cell resistance R_{sol} of 2.3 Ω is measured.

These results indicate the decomposition of the protective layer after the second cycle. In the first two cycles, no side reactions were found, but the artificial layer introduces an additional resistance ^{15,40}, creating an overpotential during lithiation and an increased R_{ct} in the slow regime. From the third cycle on, the lithiation voltage increases, indicating a decreased overpotential. Also, the R_{ct} drops down by a factor of five, indicating the dissolution of the protective layer again. However, side reactions are observed now, similar to the uncoated silicon electrode ^{25,31}. The charge difference between lithiation and subsequent delithiation is higher than the values reported for the uncoated silicon ²⁵. Becker *et al.* even found an increase in the Coulombic efficiency for the coated silicon electrode ¹⁷. Structural data is, therefore, necessary for a complementary view.

Structural analysis.

The results of the *operando* NR will be discussed now for further structural data. A 6-layer system was chosen to model the neutron reflectometry data since this system exhibits the lowest residuum (fig. S1), and no further significant residuum decrease was achieved by adding more layers. The six layers are composed of three lithiated layers and three SEI-layers (silicon oxide, aluminum oxide, conventional SEI-layer). Thicknesses of zero were also allowed to disable the layer, and an overlapping SLD-range can merge two layers or cancel out the SEI-layer due to a low SLD-contrast to the electrolyte.

Figure 4 shows the SLD-profiles obtained from the fits of the neutron reflectivity data. The fitting procedure is described in the experimental part. The figure consists of four parts. Part A shows the SLD map over the whole depth-range, whereas B is a zoom-in onto the Si-electrolyte interface. Part C represents the charge obtained from the SLD-profile and the charge estimation based on the electrochemical data. Part D shows the voltage profile. The whole *operando* experiment is split into seven sections (numbers 0 to 6), which indicate the cycle number. Additional figures showing specific cycles are shown in the supplementary information (figure S3 – S5)

Section 0 represents the **virgin state**, recorded during the initial OCV-period. Similar to the results from XRR, no smooth layer can be found but a rough SEI-layer on top of the silicon. The SEI-layer has a total thickness of approximately 8 nm, which is close to the 6.5+1.8 nm (AlOx + SiOx) obtained in the pre-characterization. No additional layers can be found initially. However, after several hours the thickness of this SEI-layer increases, indicating the growth of an additional layer on top of the protective coating. Cao *et al.* ³¹, Seidlhofer *et al.* ²², and Veith *et al.* ³⁰ also observed this phenomenon for uncoated silicon electrodes. At the end of the OCV-period, the additional SEI-layer is 3 nm thick, which is approximately 5 times thinner than reported elsewhere for the uncoated electrode ²⁵. DeCaluwe *et al.* did not observe an SEI-layer on their aluminum oxide coated silicon wafer ¹⁸. The SLD-value of the electrolyte was determined from the total reflection edge and is $3.76 \cdot 10^{-4}$ /nm^{2 20}.

Section 1 corresponds to the **first cycle**. No plateau at elevated voltages can be found and the cell voltage drops down to slightly negative values (-5 mV) after 3 minutes. The slightly negative cell voltage is a consequence of the increased resistance of the artificial layer, causing an overpotential. The lithium plating is possible at this voltage but was not observed. Instead, the growth of a lithium-rich zone within the silicon was found, as shown in fig 4A and also already found elsewhere^{22,25,30,31}. We defined the lithium-rich zone as SLD < $0.5 \cdot 10^{-4}$ /nm² or more than 1.2 Li per Si due to the continuous transition from one layer to the other. The lithiated layer grows to a maximum extent of 470 nm after 3 h. In total, 2.7 C of lithium were stored in the silicon, which matches the theoretical expectations.



Figure 4: Structural results obtained during the *operando* NR experiment. **Part A:** SLD-map obtained from the fit of the NR-data. **Part B:** Zoom-in of part A to the surface of the silicon. **Part C:** charge expected by the voltage-curve (black) and the charge within the silicon calculated from the SLD-profile (red). The charge calculation is described in the experimental part. **Part D:** Voltage-curve of the sample. OCV-periods are denoted in black, the galvanostatic cycling is drawn in red. The EIS-measurements are indicated in green. The dashed lines indicate the beginning of a cycle.

The initial SEI-layer, consisting of the silicon oxide layer, the artificial aluminum oxide layer, and the additional SEI-layer grown in the virgin state, shrinks to a thickness of 5 nm. This is lower than the initial SEI-layer thickness, indicating the loss of SLD-contrast due to the lithiation of the silicon oxide layer. This shifts the defined electrode surface from the Si/SiO_x interface to the SiO_x/AlO_x interface Such a lithiation of the native silicon oxide was already reported by Seidlhofer *et al.*²² and also in our previous work ²⁵. However, we do not observe a dedicated layer of lithiated silicon oxide LixSiOy, which was found elsewhere ^{41–43}. Here the limited contrast to the underlying lithiated silicon disables the detection of such a layer using reflectometry. No differences in the aluminum oxide layer are observed during lithiation, as already reported by DeCaluwe *et al.* An intermediate part can be found between the SEI-layers and the lithiated silicon, which models the transition region between both and exhibits a SLD-value around 2.5 x 10⁻⁴/nm². Furthermore, the lithiated zone can be subdivided into two distinct regions, (SLD > 0.5 x 10⁻⁴/nm² for the low-lithiated zone, SLD < 0.5 x 10⁻⁴/nm² for the lithiated zone), separated by a sharp interface.

The delithiation starts with a shrinkage of the lithiated zone. Approximately in the middle of the delithation process, the lithium concentration decreases. A thin lithiated region is preserved within the silicon, corresponding to 0.5 C of lithium trapped within the electrode, as already observed by Jerliu *et al.* and Rehnlund *et al.* ^{32,33}.

DeCaluwe *et al.* assigned the decreased SLD-value of the silicon after delithiation to the formation of pores ¹⁸. However, the charge calculated from the SLD-profile matches the expected charge, which is a strong hint for residual lithium. The OCV of nearly 2 V would indicate a complete delithiation of the electrode. However, the SEI-layer on top of the silicon may influence the potential measurement and lead to an additional diffusion barrier, which is indicated by the increased charge transfer resistance. Previous experiments for uncoated silicon wafers also showed a lower fraction of residual lithium ^{22,25,30}. The lithium transport may be hindered by the additional coating layer. A SEI-layer growth can be observed, resulting in a final thickness of 9 nm. This value is lower than reported elsewhere for the uncoated system^{25,30}. After delithiation, the native oxide layer does not reappear, as already described by Seidlhofer *et al.* and in our previous publication ^{22,25}

The **second cycle** (part 2) shows a similar behavior as the first cycle. No side reactions can be found and the lithiation starts immediately. Again 2.7 C of charge are inserted into the silicon, resulting in a total amount of 3.2 C due to the trapped lithium. This number was also expected by the electrochemical data. The subdivision of the lithiated zone in two distinct regions with a sharp interface can be found again.

During delithiation, 2.2 C of charge is extracted from the silicon, leaving another 0.5 C trapped in the electrode. The total amount of trapped lithium increases, therefore, to 0.9 C. At the end of the delithiation, an additional SEI-layer appears, which has a SLD-value around 1.6 x 10⁻⁴/nm². This is a decrease compared to the previous cycle. The insertion of lithium seems implausible since the charge within the silicon matches the theoretical expectations. Therefore, a volume increase or the growth of an organic SEI-layer can be assumed. Both explanations would imply a malfunction or degradation of the artificial SEI-layer. The SEI-layer shows a final thickness of 6 nm, which is less than the value of the previous cycle and indicates the decomposition of the artificial layer.

The voltage plateau at the initial part of the **third cycle** (part 3a) does not change the SEI-layer found before, but a slight contraction of the SEI is observed during the subsequent OCP. The results of the EIS-measurements indicate the partial decomposition of the layer. A lack of contrast prevents the observation of further morphology changes here. According to Ha *et al.*, moisture may be the reason for the side reactions ³⁶.

As a consequence of the voltage plateau, the current was increased to 500 μ A (part 3b). Again, a voltage plateau was observed, but the voltage decreases slowly this time. Beattie *et al.* observed a similar irreversible high voltage capacity but for tin electrodes ³⁵. This irreversible capacity may originate from electrolyte impurities, as shown by Kawamura *et al.* ⁴⁴. The silicon electrode is not coated anymore by the protective layer and its high chemical reactivity ⁴⁵ leads to side

lithiation cycle	#1	#2	#3	#4	#5	#6
highly lith. Layer in nm	120	150	360	430	490	450
ratio Li/Si	2.4	2.6	1.7	2.3	2.7	1.8
thickness lith. zone in nm	470	470	1200	1250	1260	1300
stored charge in C	2.7	3.2	8.0	9.7	10.7	9.5
thickness SEI-layer in nm	5	5	10	13	12	13
Fast R_{ct} in Ω	6.7	8.1	2.9	1.4	1.6	1.5
Slow R_{ct} in k Ω	0.65	0.60	0.25	0.17	0.17	0.36
R_{sol} in Ω	1.8	1.9	1.8	1.8	1.9	1.9

Tab. 1: Parameters characterizing the lithiated states

reactions. Once the voltage drops below 300 mV, lithium insertion into the silicon starts and the final lithiation voltage is 30 mV, which is slightly lower than for the uncoated silicon ^{22,25}. The resulting profile does not exhibit the sharp separation of highly- and lowly-lithiated layers anymore.

Instead, this transition broadens. The lithium's penetration depth into the silicon increases to approximately 1200 nm, while the lithium concentration decreases. 14 C of charge are involved in side reactions. After delithation, 4 C of charge remain in the silicon electrode. The SEI-layer exhibits a thickness of 15 nm but has little contrast against the electrolyte. The SEI-layer thickness is still lower than reported elsewhere for the uncoated silicon ^{25,30}. The high amount of trapped charge may be a consequence of the impeded lithium transport through the SEI-layers. However, such a mechanism was not observed before ^{22,25,30}. The lithiation voltage increase indicates again the artificial coating layer's decomposition, which introduced an overpotential in the first two cycles.

Cycles 4 to 6 (parts 4, 5, and 6) show similar characteristics. Two additional high voltage plateaus are observed at 1.5 V and 0.7 V. For the second plateau, a SLD-decrease of the SEI-layer is found, whereas no morphology change is observed at the first plateau. This is in contrast to our preceding work, where only the first plateau was observed and assigned to morphological changes of the SEI-layer ²⁵. The maximum of the lithium concentration increases in the fourth and fifth cycle, while it decreases again in the last cycle due to the decreased current. The maximum depth stays nearly constant. The SEI-layer exhibits a cyclic behavior. During lithiation, the thickness and the SLD of the SEI-layer decrease slightly. The subsequent OCV-period leads to a SLD-increase again, followed by a thickness decrease during delithiation. The OCV-period in the delithiated state leads to a thickness increase of the SEI-layer, comparable to findings of Veith *et al.* ³⁰. The trapped lithium also increases cyclewise, leaving 6.4 C of lithium in the silicon after the sixth cycle. Tables 1 and 2 summarize the most critical parameters for the lithiated and delithiated states, respectively.

delithiation cycle	VS	#1	#2	#3	#4	#5	#6
Ratio Li/Si	0	0.3	0.3	1.0	1.0	1.1	1.0
thickness lith. zone in nm	0	300	350	760	900	960	970
trapped charge in C	-	0.5	0.9	4.0	5.0	6.0	6.4
thickness SEI in nm	11	9	6	15	16	16	18
Fast R_{ct} in Ω	15	118	292	5789	7409	4147	4266
Slow R_{ct} in $k\Omega$	355	239	296	217	180	242	241
R_{sol} in Ω	1.9	1.9	1.9	2.0	2.0	2.1	2.1

Tab. 2: Parameters characterizing the delithiated states

Conclusion

The lithium insertion into a crystalline silicon wafer coated with an artificial aluminum oxide layer was studied. *Operando* NR was used for morphological analysis, while *in-situ* EIS was used to probe the sample's electrochemical properties. In total, six cycles were investigated under *operando* conditions.

- The aluminum oxide layer suppressed side reactions on the silicon surface successfully in the first two cycles. However, despite the suppression of the electrolyte's decomposition, the presence of aluminum oxide on the Si surface introduces higher charge transfer resistances.
- After two cycles, the artificial layer lost its protective properties. Additional voltage plateaus associated with parasitic side reactions are observed. A morphology change on the surface of the silicon can be found, indicating the decomposition of the protective layer. This is in contrast to other work, where aluminum oxide has proven its beneficial properties also over many cycles.
- During the lithiation process itself, no side reactions and no leakage current is observed.
 All lithium ions generated at voltages < 300 mV participate in the growth of the lithiated zone, but 15 20 % of the inserted charge is trapped within the silicon after delithiation.
- The SEI-layer shows cyclic behavior. During lithiation, the layer shrinks, whereas it grows during delithiation. This process leads to a net growth with cycle number.

A detailed analysis of the degradation of the artificial layer was not possible due to a lack of SLDcontrast. Thus, more studies are necessary to ensure the durability of the film. Also, variations of the isotopes within the electrolyte may generate valuable insights into the formation mechanism of the SEI and the lithiation mechanism of the aluminum oxide film.

Experimental

The employed *operando*-cell is shown in fig. 5. A detailed description is given in ²⁵. A single crystalline silicon wafer (phosphorous-doped, 100-orientation, 6 cm diameter, 1 cm thickness) was used as an electrode. Prior to the deposition, the wafer was cleaned with a cascade of different solvents (EXTRAN MA01 from Merck, 1:100 with ultrapure water, plain ultrapure water, Ethanol p.a. with ultrapure water 1:1, Acetone (purity > 99.5 %), 2-Propanol (purity > 99.8%)). The protective layer was formed by depositing 3.0 nm (0.1 nm/s) of aluminum by electron beam evaporation in a custom-made deposition chamber. A base pressure of $2 \cdot 10^{-7}$ mbar was measured during the deposition process. The emission current was 55 mA at a beam power of 0.6 kW. The storage of the sample in air enabled the formation of aluminum oxide.



Figure 5: Employed *operando* cell. A detailed description is given in ²⁵. The most essential parts are indicated.

The pre-characterization was done using an in-house developed X-ray reflectometer (Cu-K α -radiation, angular resolution 0.001°).

Just before the experiment, the electrolyte was prepared by mixing Ethylene carbonate (Solvionic, H2O < 20 ppm, battery grade) with deuterated Dimethyl carbonate (abcr, deuteration grade >99.84 %, water < 0.04 %) in a 1:1 ratio by volume. LiPF₆ salt (Sigma Aldrich, battery grade, 99.99% trace metals basis) was added afterward, resulting in a one-molar solution. The initial neutron measurements revealed a SLD-value of the electrolyte of 3.76.10⁻⁴/nm². This can be calculates from the total reflection condition in Snells law of refraction, since the SLD of the incoming media is known (silicon, 2.07·10⁻⁴/nm²). The cell was assembled 6 h before the experiment in a helium-filled glovebox (H2O, O2 < 10 ppm). A metallic lithium sheet was used as counter-electrode, small parts of lithium oxide were removed with a scalpel. Porous polymer foil (Celgard 2700) served as a separator. An initial EIS-measurement revealed a cell resistance of 1.7 Ω , of which approximately 0.8 Ω originate from the electrolyte itself ²⁹. The frequency range probed here was 1 MHz to 0.1 Hz, 15 points/decade, 3 mV rms of the excitation voltage signal. All electrochemical measurements were done using a GAMRY interface 1000 potentiostat. Initially, an OCV-period of 13 h was conducted to ensure the wetting of all cell parts. After the OCV-period, another EIS was measured with a shorter frequency range (100 kHz to 0.1 Hz), followed by cell cycling. Here a current of 250 µA was used initially. The lithiation continues for 3 h once the voltage dropped below 250 mV. After the lithiation, a 2-h-OCV period followed, with EIS-measurements at the beginning, in the middle, and at the end. Afterward, the delithation takes place up to a cut-off voltage of 3.0 V, again followed by a 2-h OCV period and the EIS in between. In the third, fourth, and fifth cycle, the current was increased to 500 μ A. The last cycle was done with 250 μ A again.

The EIS-data were evaluated using the equivalent circuit shown in fig. S2. A custom-made Mathematica-script was used to analyze the data by minimizing the relative deviation between modelled impedance and measured data. A selection of results are shown in the supplementary information (figure S7). An Integration of the time constant distribution function gives the charge transfer resistance. The resistance arising from processes faster than 1.5 s (integration from small relaxation times up to 1.5 s) is denoted as _{Rct, fast}. The complementary definition is used for R_{ct, slow}. Neutron measurements were carried out at the OFFSPEC-instrument at ISIS Neutron and Muon source ^{46,47}. A polychromatic beam (0.15 to 1.4 nm wavelength) was used, resulting in a q-range from 0.083 to 0.99/nm for the *operando*-scans and 0.083 to 2.49/nm for the initial virgin state scan. The *operando*-scans took roughly 6.75 minutes each. The Mantid software package was used for data reduction ⁴⁸. The data analysis was performed with a custom-made python script, which employs parts of the refnx-software for reflectivity calculations ⁴⁹. The differential evolution algorithm was employed ⁵⁰, which was implemented already in the Scipy library ⁵¹. A sum of four residues was taken to find the best solution:

The first residuum χ_{refl} takes the logarithmic difference of the experimental data and the reflectivity of the model, weighted by the experimental errors. The second residuum χ_{charge} takes the difference of the charge found within the silicon-based on the NR-results and the charge estimated from the electrochemical data. For this estimation, the integration of the current below 300 mV was done during lithiation. For the delithation, the current integration was done regardless of the voltage. The charge within the silicon was determined from the SLD-profiles. The SLDvalue of a mixed phase can be calculated by the scattering length b of the individual compounts, multiplied by their number density within the phase. Therefore, the stochiometric ratio x of a LixSi phase can be calculated as ^{22,52}:

$$x = \frac{b_{Si} + xb_{Li}}{x \cdot \Delta V + V_{Si}} \tag{1}$$

 V_{si} denotes the volume per silicon atom (0.213nm³) whereas ΔV denotes the volume increase per inserted lithium atom (0.147 nm³)^{22,53}. An integration along the depth and a multiplication with the geometric surface area of the electrode yields the stored charge.

The third residuum $\chi_{profile}$ was the difference between neighboring SLD-profiles. Up to three profiles before and after the currently analyzed profiles are chosen as reference. The difference between the current profile and the other is calculated and weighted with a Gaussian distribution to consider the increased time difference.

The last residuum χ_{bin} was a binary switch to discard non-meaningful SLD-profiles, which contain artifacts from roughnesses higher than the layer thickness. Also, profiles with a higher lithium content in the bulk of the silicon compared to the surface region were discarded since lithium is introduced from the surface. This is in line with profiles found elsewhere ^{22,25}.

The data analysis was done over 35 rounds. In the first round, the third residuum was discarded to generate an initial solution. Afterward, the usage of the third residuum leads to a smoothening of the profiles, as indicated in fig. S6. The smoothening did not lead to an increase of the other residues. After 28 rounds, a subseries was replaced by manually selected results, which seem to be more meaningful. The whole dataset was analyzed further for 7 rounds. At the final solution, the fraction of the different residues were: $\chi_{refl} \sim 0.763$, $\chi_{charge} \sim 0.002$, $\chi_{profile} \sim 0.235$. $\chi_{bin} \sim 0$.

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/xxx/ Optimization of the SLD-model, Equivalent circuit used for the analysis of the EIS-measurement, SLD-pattern of the virgin state up to the second cycle, SLD-pattern of the third cycle, SLD-pattern of the fourth to sixth cycle, Evolution of the SLD-map during fit-rounds, Selection of the EIS analysis results and the corresponding fits.

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Table of Content (TOC):



Supporting Information

Solid Electrolyte Interphase Layer Formation during Lithiation of Single Crystal Silicon Electrodes with a Protective Aluminum Oxide Coating

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Figure S1: Optimization of the SLD-model. Four different layer-numbers were tested against an intermediate lithiated state. A 6-layer model showed the lowest residuum and was therefore chosen to analyze the data.



Figure S2: Equivalent circuit used for the analysis of the EIS-measurement. The distribution of relaxation times $\gamma(\tau)$ is split into a fast ($\tau < 1.5$ s) and a slow ($\tau > 1.5$ s) part.



Figure S3: SLD-pattern of the virgin state up to the second cycle. On top the SLD-map of the whole depth is shown, in the middle a zoom-in to the surface. The voltage is shown at the bottom. Dashed lines indicate the beginning of a cycle. The white rectangle indicates the decomposition of the artificial SEI-layer.



Figure S4: SLD-pattern of the third cycle. On top the SLD-map of the whole depth is shown, in the middle a zoom-in to the surface. The voltage is shown at the bottom. Dashed lines indicate the beginning of a cycle. The grey rectangle indicates the decomposition SEI-layer, which delays the lithiation process.



Figure S5: SLD-pattern of the fourth to sixth cycle. On top the SLD-map of the whole depth is shown, in the middle a zoom-in to the surface. The voltage is shown at the bottom. Dashed lines indicate the beginning of a cycle.



Figure S6: Evolution of the SLD-map during fit-rounds. On top, the SLD-map after the initial fitting is shown without taking neighboring profiles into account. The observed differences between the profiles are not meaningful since they result from a continuous data-acquisition (*operando*-measurement). Therefore the neighboring profiles were taken into account. The resulting SLD-map after 3 and 10 cycles is shown in the middle and at the bottom, respectively. The reflectivity- and charge-residuum do not increase significantly. The white stripes denote the absence of reflectivity data due to beam off periods.





Figure S7: Selection of the EIS analysis results and the corresponding fits.