Low temperature atomic layer deposited magnesium oxide as a passivating electron contact for c-Si based solar cells

Ganna Chistiakova, Bart Macco, Lars Korte

Abstract **-In this work, we explore magnesium oxide (MgO) as electron-selective contact layer in silicon heterojunction solar cells. We report on the successful deposition of MgO layers by atomic layer deposition (ALD) at low temperatures ≤200 °C using Bis(ethylcyclopentadienyl)magnesium (Mg(CpEt)2 and H2O as precursors. Depositions were carried out on bare c-Si wafers and c-Si wafers with an intrinsic amorphous hydrogenated silicon (i-aSi:H) passivation layer. The resulting interfacial properties, surface passivation quality and contact resistivity were investigated. Upon initial deposition of MgO on an i-aSi:H/c-Si stack, the c-Si surface passivation degrades drastically. However, with an additional annealing step of 5 minutes at 200-250 °C it is possible to reverse the degradation and even to achieve charge carrier lifetimes in excess of those achieved with an i-aSi:H alone. Furthermore, we show that MgO forms an Ohmic contact with both MgO/i-aSi:H/c-Si and MgO/c-Si stacks, and we demonstrate solar cells using both types of stacks as electron contact layers.**

Index terms**-Atomic layer deposition, electron selective contact, magnesium oxide, crystalline silicon solar cells, passivation.**

I. INTRODUCTION

In the development of crystalline silicon (c-Si) solar cells, nanolayer engineering for surface passivation and selective carrier extraction has become an increasingly important topic. For homojunction cells, which have carrier-selective contacts based on highly *p*- and *n*-doped Si regions, the implementation of surface passivation schemes has been pivotal in achieving higher efficiencies. A prime example is the introduction of Al_2O_3-based passivation layers at the rear side of the wafer, i.e. in PERC cells, which is now becoming the industrial standard[1]. For silicon solar cells based on heterojunctions, thin films not only provide surface passivation, but should also allow for selective extraction of carriers. A conventional heterojunction approach involves the deposition of an intrinsic hydrogenated amorphous silicon (a-Si:H) passivation layer, followed by a *n*- or *p*-doped a-Si:H layer for carrier selectivity. More recently, also carrier-selective contacts based on a passivating ultrathin (~1.5 nm) SiO_2 layer followed by an *n*- or *p*- doped poly-Si layer have been shown to yield excellent solar cell performance[2]. Besides these heterojunctions based on doped silicon layers, there has also been an increasing interest in dopant-free metal oxide layers. Rather than on doping, these layers rely on asymmetric band valence- and conduction band offsets at the oxide/*c*-Si interface to achieve carrier selectivity, which is often accompanied by an additional induced band bending [3], [4]. This approach can have some potential benefits, such as enhanced transparency, no need for dopants, and additionally ease-of-processing as some of these selective layers do not require a dedicated passivation layer. Although the dopant-free approaches do not yet reach the >25 % efficiency level of the doped silicon layers[5], solar cell with metal oxide layers have in a span of a few years already demonstrated efficiencies in excess of 22 %[6]. Also more and more carrier-selective materials based on metal oxides (TiO_2[6], Nb_2O_5[7], MO_3[8]), metal nitrides (TaN[9]) and metal fluorides (LiF[10]) are being developed for device applications. Further optimization and also further exploration of novel carrier-selective contacts therefore remains of importance to chart the potential of this dopant-free approach. One of the possible candidates to consider is magnesium oxide (MgO). Magnesium oxide has a work function of 4.2 eV[11], which makes it a suitable material for the electron contact in c-Si based devices[3]. Recently, the successful implementation of MgO thin layers as stand-alone passivation and electron transport layers for n-type c-Si wafers[8], [12], [13], and in combination with aluminum oxide ($Al_xMg_{1-x}O_y$) as

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passivation layer for p-type c-Si wafers[14] have been shown. Devices with 1-2 nm thin MgO electron-selective contacts, prepared by e-beam or thermal evaporation, have been reported. These devices showed moderate improvement of the passivation with MgO layer, however had a good contact resistance in the range of 18-40 mΩcm^2 for a MgO thickness of ~1 nm. The main issue with implementing MgO layers is a trade-off between passivation and contact resistance: By increasing the MgO layer thickness it is possible to achieve higher passivation quality, but at the same time the contact resistance increases drastically, due to the insulating nature of the MgO layers. Therefore, an optimal thickness has to be established.

Additionally, in common deposition techniques such as chemical beam deposition[15], metal-organic chemical vapor deposition[16], [17] or chemical vapor deposition[18], the growth of MgO layers demands high deposition temperatures. In order to decrease the deposition temperature without sacrificing layer properties, atomic layer deposition (ALD) can be considered, which has the additional benefits of high uniformity, the possibility to control the layer thickness at the monolayer scale and is widely used in industry. However, most ALD precursors for MgO have a working temperature window above 200°C[19], [20]. Such deposition temperatures can be considered for direct c-Si wafer passivation, but they are incompatible with i-aSi:H passivation layers due to their limited thermal stability. However, for a process with lower temperature requirements, it would become possible to consider magnesium oxide not only as a stand-alone passivation layer, but as part of the passivation stack in silicon hetero-junction solar cells, combining i-aSi:H and MgO layers into a passivation/electron transport layer stack.

To this end, we investigate MgO layers produced with a water-based ALD process using Bis(ethylcyclopentadienyl)magnesium ($Mg(CpEt)_2$). This precursor was shown to be a suitable precursor for the growth of high quality MgO layers in the deposition temperature range 125-200 °C, and it can be used in ALD using water as oxidizing agent [21]. We investigate such an ALD process for MgO thin film deposition, with a focus on obtaining well-passivated interfaces for MgO/c-Si and MgO/i-aSi:H layer stacks. We evaluate the surface passivation and electrical contact performance of these stacks in order to assess their potential as electron-selective contacts in c-Si based devices. Additionally, X-ray photoelectron spectroscopy (XPS) measurements were conducted in order to obtain information about the chemical state of the investigated MgO layers, and about the dependence of the layer composition on deposition temperature and post-deposition annealing treatment. Finally, as a proof of concept, solar cell devices implementing these ALD MgO layers as electron-selective contacts are presented.

II. Experimental methods

MgO films were deposited by thermal ALD in an Arradiance GEMStar XT 6-8 ALD reactor. $Mg(CpEt)_2$ was used as precursor, which was held at a temperature of 80 °C. N_2 as carrier gas and water as reactant were used. The ALD cycle consisted of a 1 second pulse of $Mg(CpEt)_2$, 10 seconds of first purge step with N_2, a 750 ms pulse of water, and 10 seconds second purge with N_2. The deposition temperature was varied in the range of 125-200 °C. In this temperature range, no notable changes in the growth per cycle were observed. Therefore, this temperature range can be considered as a suitable temperature window for the ALD process. The standard deposition temperature was fixed at 150 °C.

For the MgO/c-Si and MgO/i-aSi:H interface investigation, polished n-type c-Si wafers, float zone, with <100> surface orientation, a resistivity of ~1-3 Ω cm, and 280 µm thickness were used. Prior to deposition, wafers were cleaned with the standard RCA process[22] and afterwards dipped in 1% HF for 2 minutes in order to remove the wet-chemical oxide grown at the surface. To investigate the c-Si surface passivation by MgO/i-aSi:H stacks, 5 nm i-aSi:H layers were deposited using plasma enhanced chemical vapor deposition (PECVD) prior to the ALD deposition of the MgO layer. Deposition parameters for i-aSi:H layers were: flow rates of 13 sccm silane (SiH_4) and 7 sccm H_2, plasma excitation frequency of 13.56 Mhz, power density of 45 mW/cm^2, and a deposition temperature of 185 °C. Afterwards, the i-aSi:H layers were annealed for 20 minutes at 200 °C in N_2 atmosphere in order to improve the passivation quality and to exclude additional annealing effects for the interface during the MgO layer deposition at elevated temperatures and/or further post-deposition annealing steps.

To assess minority carrier lifetimes, transient photoconductance decay (TRPCD) and quasi-steady-state photo conductance (QSSPC) measurements were conducted on a Sinton Consulting WCT-100 set-up. Investigated samples had symmetrical layer stacks on both sides of the wafer. Minority carrier lifetime data was extracted at an injection level of 10^{15} cm^{-3}. The full lifetime *vs.* injection level data sets, $\tau(\Delta p)$, were further analyzed using a semi-analytical simulation model in order to separate the influence of field-effect passivation from defect passivation for the investigated layer stacks. This was done by fitting with the semi-analytical lifetime model to the measured $\tau(\Delta p)$, using the effective fixed charge Q_i and concentration of interfacial defects D_{it} as fit parameters. Depending on features of the lifetime curve, it is possible to discern between D_{it} and Q_i. D_{it} shifts the curve

upwards or downwards, while maintaining the shape of the curve. At the same time, changes in fixed charge density have a strong impact on the curve shape, influencing carrier lifetimes mostly at low Δp since field effect passivation (due to high Q_i) is only effective in low injection. The biggest ambiguity is the sign of the curve. For $Q_i < 10^{12}$ cm^{-2}, it is possible to deduce the sign from the curve shape itself. For higher charges, additional SPV measurements were used to determine the sign of the charge, and the lifetime fit was then initialized with a high charge of the appropriate sign. See [23], [24] for details.

Contact resistivity measurements were performed using the Cox and Strack method [25] using the same substrate c-Si wafers. At the front side, MgO layers of varied thickness were deposited on top c-Si, or i:aSi:H/c-Si layer stack. Afterwards, on top of the MgO layer, 2 µm thick circular aluminum contact dots (diameter 0.2-2 cm) were thermally evaporated through a shadow mask using a Creavac 3000 evaporator. On the rear side of the structure a 10 nm titanium/500 nm silver metal stack was thermally evaporated. This yields an Ohmic contact to the c-Si wafer and is assumed to contribute negligibly to the total resistance of the sample.

Film thicknesses were extracted from spectroscopic ellipsometry measurements using a Sentech SE850 UV-Vis ellipsometer (wavelength range 190-850 nm), using a Cauchy model for the MgO layers and a Tauc-Lorentz model for i-aSi:H layers.

XPS measurements were performed in an ultra-high vacuum (UHV) system with a base pressure in the range of 5×10^{-9} mbar, using non-monochromatized Mg K_α excitation and a ScientaOmicron Argus Cu electron analyzer. Samples were transported without breaking vacuum from the deposition tool to the XPS system through N_2 gloveboxes, and were annealed in-system at 200 °C. The analysis of XPS core level spectra was done using the software fityk[26]. Spectra were fitted using Voigt profiles with coupled Gaussian and Lorentzian line widths for the core level peaks, and a linear background was included. The change in the elemental composition was calculated, after subtraction of the fitted background, from the fitted peak areas relative to the total area of the main peaks (i.e. carbon 1s, oxygen 1s, magnesium 2p and silicon 2p).

Additionally, as a proof of concept solar cells were produced on the same substrate c-Si polished wafers. Two types of solar cells structures were considered: They have different rear sides with either a direct c-Si/MgO contact or with an i-aSi:H buffer layer, i.e. an c-Si/i-aSi:H/MgO layer stack. Both type of layer stacks received 5 minutes annealing at 200 °C after the MgO layer deposition. For both cases the front side of the device was the same and consisted of 5 nm of i-aSi:H, 10 nm p-aSi:H and 80 nm of RF-sputtered ITO layers. ITO was deposited through a shadow mask to define a solar cell area of 1 cm^2. For the reference cells the rear side stack was: 5 nm of i-aSi:H, 10 nm of n-aSi:H, 80 nm of ITO. After the sputtering step, samples were annealed for another 5 minutes at 200 °C in order to remove sputter damage. Metallization was done by thermal evaporation. The front grid consisted of a metal stack of 10 nm titanium and 1.5 µm silver and was defined by using a shadow mask. The rear side metallization consisted of a blanket layer of 1 µm aluminum; for the reference cells the rear side metallization consisted of a blanket layer of 10 nm titanium and 500 nm silver.

III. Results and Discussion

A. *Growth behaviour of MgO layers*

We begin by evaluating the growth behavior of ALD MgO layers on c-Si and i-aSi:H substrates, as shown in Fig. 1. For both cases a linear growth as well as a slight growth delay is observed: The linear fits cross the abscissa at around 4 cycles for the series on c-Si and at 7 cycles on a-Si:H. For the i-aSi:H substrate, this delay is possibly higher due to the surface passivation with silicon-hydrogen bonds, which hinders the nucleation of an MgO layer at the i-aSi:H surface during the first cycles of the deposition process[27], [28].

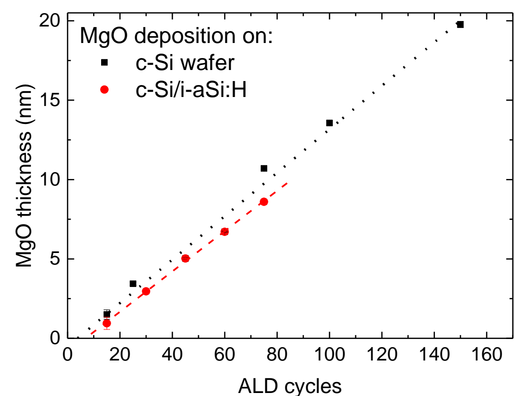

Fig. 1. Film thickness of MgO layers grown on a HF- dipped c-Si wafers (black) and i-aSi:H layers on c-Si (red), as a function of ALD cycles. Deposition temperature was set at 150 °C.

B. *Passivation quality of MgO layers as a function of layer thickness*

We now proceed to an investigation of interface properties for the c-Si/MgO and i-aSi:H/MgO layer stacks. Samples with symmetrical layer stacks on both sides of the wafer were produced in order to investigate changes of the passivation quality in terms of minority carrier lifetime upon deposition of MgO layers.

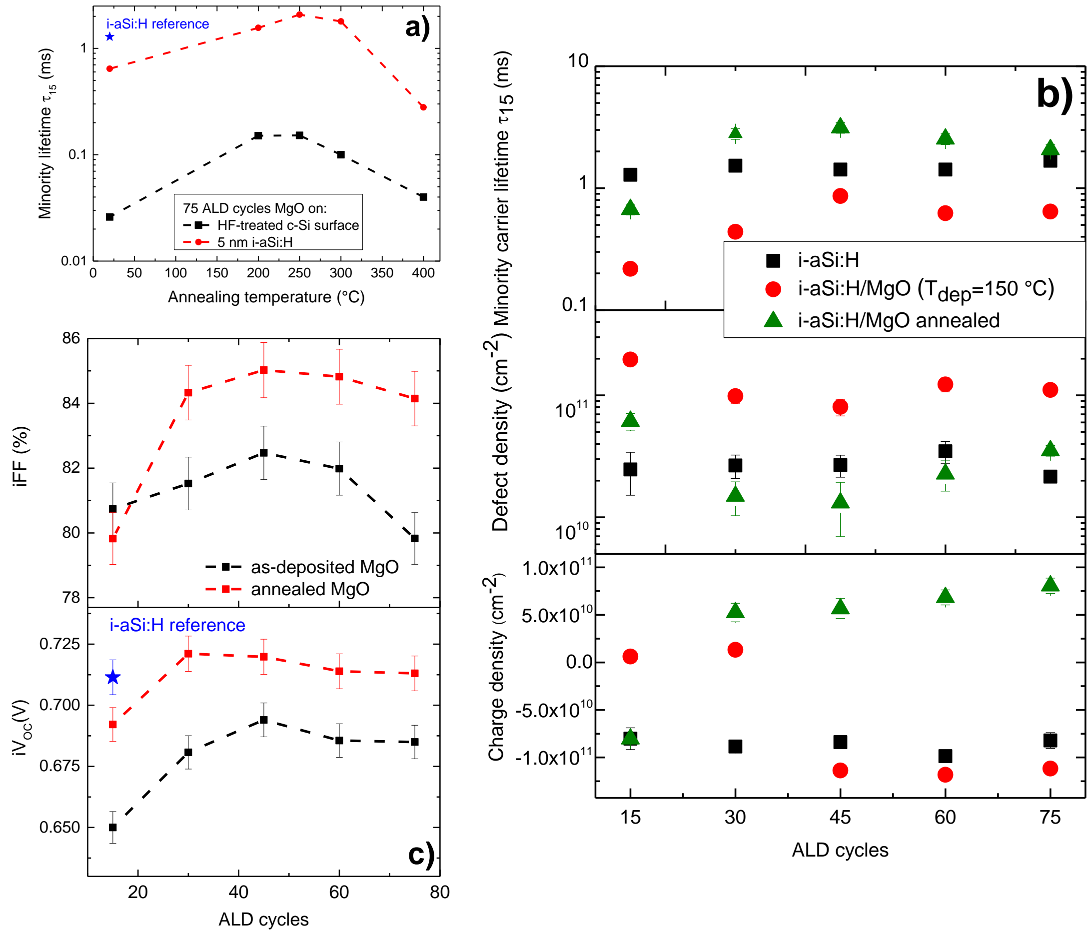

Fig. 2. (a) Effective excess minority carrier lifetime at 10^{15} cm^{-3} injection level after MgO layer deposition at 150 °C for the HF-treated c-Si wafer and i-aSi:H/MgO layer stacks on c-Si, as a function of the annealing temperature. (b) Carrier lifetime at 10^{15} cm^{-3} injection level, modelled defect densities and effective charge, (c) implied fill factor and V_{OC} for for i-aSi:H/MgO layer stacks on c-Si substrate, as a function of the number of ALD deposition cycles.

We observe that with the direct deposition of a thin MgO layer on c-Si substrates, no passivation was achieved, neither in the as-deposited state nor after the annealing steps. However, for a thicker MgO layer, i.e. after 75 ALD cycles ($d_{MgO} \approx 9.8$ nm), as is seen in Fig. 2 a, changes in the passivation quality are observable. For the as-deposited stack no passivation is observed. However, after an annealing step of 5 minutes at 200-250 °C, a slight passivation effect, yielding a lifetime of around 150 µs, is present.

A similar experiment was done with MgO deposited on i-aSi:H coated c-Si substrates. In this case, it was possible to observe significant changes in the effective lifetime with varying MgO thickness. In Fig. 2 b, the effective minority charge carrier lifetime for c-Si wafers coated with such layer stacks is shown as a function of the number of ALD cycles. Additionally implied FF and V_{OC} for such stacks are presented in Fig 2 c. It can be seen that after the direct deposition of an MgO layer on top of i-aSi:H, there is a noticeable degradation of the lifetime and iV_{OC} for all MgO layer thicknesses.

Using fits of our minority carrier lifetime model, we find that this is caused by a drastic increase in c-Si interface defect density (middle panel in fig. 2 b).

However, similar to the MgO/c-Si layer stack, a recovery of passivation and improvement beyond the initial level is observed after an annealing step at 200 °C, with the maximum increase for the sample after 45 MgO ALD cycles, which corresponds to the sample with the lowest defect density. At the same time, the total effective charge is slightly increasing

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with the number of deposition cycles. Therefore, we conclude that the main c-Si interface passivation mechanism is chemical passivation by the i-aSi:H film, which degrades upon MgO deposition. This degradation can be caused by defect generation in the a-Si:H during MgO deposition, by formation of a defective MgO/i-aSi:H interface, or by defects in the MgO layer itself. After the annealing step the degradation can be reversed: according to the lifetime fitting results, the defect density at the interface to the c-Si wafer then drops to levels below the initial ones (middle panel of Fig. 2b). The existence of an optimal MgO layer thickness for the passivation is similar to results found for some other metal oxides, such as TiO_2[29]. Furthermore, it is interesting to note that the fixed charge reverses its sign: While it is rather small and negative, ~-1x10^{11}/cm² after i-aSi:H deposition, it increases to > +5x10^{11}/cm² after MgO deposition and anneal, for all MgO thicknesses except the thinnest (15 cycles). This indicates, that MgO/i-aSi:H stacks are indeed suitable as electron contact layers, since the positive fixed charge leads to a downwards band bending, i.e. an electrical field that attracts electrons to this contact. It is not fully clear why the fixed charge changes its sign. It appears that after 15 cycles, the MgO layer is not yet fully closed, and that the intermediate SiO_x, which is formed at the interface between i-aSi:H and MgO layer therefore plays the dominant role for the values of D_{it} and the sign of Q_i. Another possibility that upon annealing, the Mg-OH bonds are substituted with Mg-O [30]. This possibly causes the decrease in D_{it} and change of Q_i sign. This matter will be discussed further when we come to the XPS results presented below.

Thus, the annealing step is needed after the MgO layer deposition in order to improve the passivation quality by decreasing the defect density at the interface and reversing the sign of the charge. Next, we optimized the annealing temperature in order to achieve the highest passivation improvement. Fig. 2 a) compares the minority carrier lifetimes as a function of the annealing temperature for both layer stacks. As expected for the MgO/i-aSi:H layer stack, the minority carrier lifetime values are decreasing at annealing temperatures above 300 °C due to the degradation of the i-aSi:H layer caused by hydrogen effusion[31]. The MgO/c-Si layer stack shows a similar trend, with the total degradation of the effective lifetime at annealing temperatures above 300 °C.

C. Dependence of MgO passivation quality on ALD deposition temperature

Another important parameter to consider is deposition temperature. As mentioned before, the temperature window for our MgO ALD process is ~ 125-200°C. Therefore, in this temperature range, it is possible to expect the highest precursor utilization during the deposition process. We proceed by investigating the passivation properties for the MgO/i-aSi:H layer stack with varied deposition temperature of MgO layers.

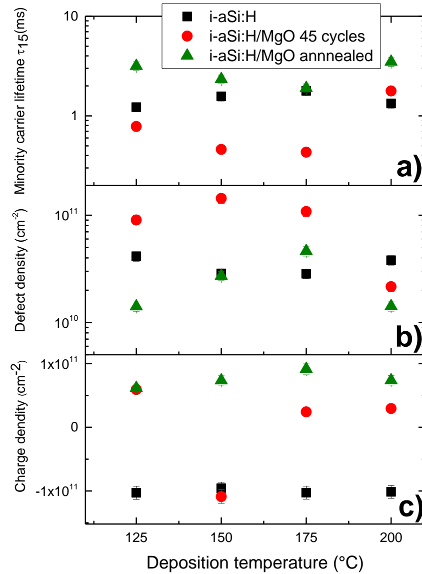

Fig. 3. (a) Effective excess minority carrier lifetimes at 10^{15} cm^{-3} injection level, (b) c-Si interface defect density, (c) fixed charge density after 45 cycles of MgO layer deposition on 5 nm i-aSi:H/c-Si, as a function of the ALD deposition temperature.

Fig. 3 shows the effective excess minority carrier lifetime for MgO/i-aSi:H/c-Si structures as a function of the deposition temperature for as-deposited samples as well as after the annealing step at 250 °C for 5 minutes. We observe a change of effective lifetime with deposition temperature. For the samples deposited at a temperature below 200 °C the minority carrier lifetime drastically degrades after the initial MgO layer growth. In contrast, the sample deposited at 200 °C shows an improvement that can probably be assigned to a further beneficial effect of i-aSi:H annealing during the ALD process. All lifetimes could be recovered or improved by the short annealing step at 250 °C. Interestingly, lifetimes are highest after annealing for the lowest and highest ALD temperatures, whereas for the i-aSi:H/c-Si samples, i.e. prior to MgO deposition, the lifetime minimum is at an intermediate temperature of 175°C, which corresponds to the maximum of defect density. It is possible to see that for deposition temperatures of 175-200 °C, the initial fixed charge sign remains the same after the direct deposition and annealing. However, after the annealing sign is the same for all samples, and quantitatively the charge is comparable for all samples.

D. XPS analysis of ALD MgO layers

To shed light on the physical reasons for these findings, it is important to identify changes at the MgO/Si interface upon MgO deposition and after the annealing step. Therefore, MgO/i-aSi:H/c-Si

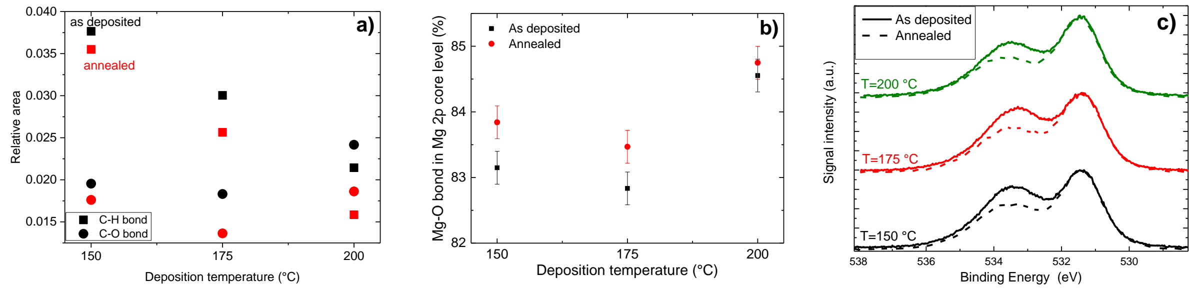

Fig. 4. a) Relative area for the components of the C 1s core level signal, relative to the total area contributed by all main core levels, b) Relative area of Mg-O bond to the total area of the Mg 2p core level signal, c) Normalized intensity of O 1s core level signal for as-deposited samples at varied deposition temperature, and after annealing at 200 °C.

samples were prepared for XPS investigations: thin layers of around 3 nm MgO (30 ALD cycles) were deposited on top of an i-aSi:H layer at temperatures in the range of 150-200 °C. Such thin layers of MgO allow to observe X-ray excited photoelectrons not only from the MgO film, but also from the underlying i-aSi:H layer. However, at the same time, the MgO film is thick enough to behave as a fully formed layer. All samples were measured as-deposited and then annealed in vacuum at 200 °C for 5 minutes.

We start the XPS analysis of these samples with the C 1s core level signal. The C 1s core level signal could be fitted with two components: A peak that is assigned to C-H bonds at the binding energy around 287 eV, and a peak stemming from C-O groups at 289 eV[32]. No formation of $Mg(CO)_3$[32] in the Mg core level signal was detectable. Therefore, it can be assumed that these observed carbon bonds originate from the $Mg(CpEt)_2$ precursor residuals. In Fig. 4 a, the area of C-H and C-O bonds relative to the total area of the main core level signals is shown. The carbon concentration changes for different deposition temperatures: The relative area for both bonds decreases with the deposition temperature, and it decreases further upon annealing. However, for the sample deposited at 200 °C, the C-O signal is increased as compared to the other deposition temperatures, which could be an indication of the start of precursor decomposition.

The next core level of interest is the Mg 2p core level. It this core level, there are two clearly detectable components: Mg-(OH) and Mg-O bonds[33]. Fig. 4 b shows that for all deposition temperatures, the ratio of Mg-O bonds relative to Mg-(OH) bonds increases after the annealing step. Therefore, it is possible to conclude that with annealing the Mg-(OH) bonds are indeed substituted with Mg-O bonds[30], as surmised from the passivation/carrier lifetime data. Finally, we investigate the O 1s core level. In this signal, at least 5 components, i.e. individual peaks, are present which are hard to distinguish and difficult to assign to specific chemical bonds. The components that could be located in this binding energy range are: Mg-O, O-Si, -Mg(OH), -CO, H_2O[32], [34]. Because of this complicated peak structure and the limited energy resolution, we refrain from fitting individual peaks to this signal. However, fig. 4 c shows that for all samples after annealing, the signal intensity at higher binding energies is decreasing.

Within this sample series, we also analyzed the Si 2p core level (data shown in the SI), and have observed the presence of all four oxidation states of silicon, which indicates the presence of silicon suboxides, SiO_x with $x < 2$, at the interface between i-aSi:H and the MgO. However, no observable changes were seen in this core level upon annealing. Therefore, it can be concluded that the O-Si contribution should also be unchanged in the O 1s core level. Keeping this in mind, we can surmise that the annealing step is mainly affecting –CO and –OH groups within the MgO film, and we conclude that with the annealing step layers become more stoichiometric[35]. The annealing temperature of 200-250 °C is sufficient to break the –OH bond. Therefore, it is possible that hydrogen diffuses from MgO layer to the interface, hence the MgO layers become less defective due to less hydrogen at the surface and in the bulk. Thus, both bulk and interface passivation would be improved.

E. Contact resistivity of ALD MgO layers

Next, we evaluate the electrical contact properties of MgO/c-Si and MgO/i-aSi:H/c-Si layer stacks.

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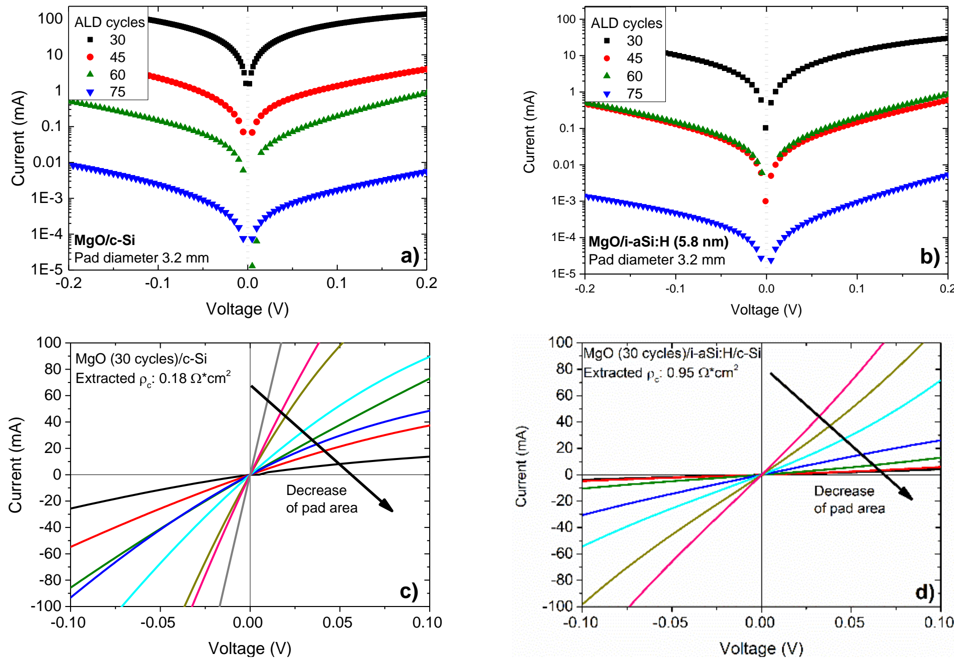

Fig. 5. J (V) characteristics for varying thicknesses of ALD MgO deposited at 150 °C on a) bare c-Si substrates, b) on top of i-aSi:H/c-Si layer stacks. J-V characteristics for varying pad diameter for the test structures after 30 cycles of MgO on c) bare c-Si substrates, d) on top of i-aSi:H/c-Si layer stacks. Samples were annealed at 250 °C before the metallization process.

Test structures using the method devised by Cox and Strack were investigated[25]. Note, that using the Cox & Strack method, we are not able to discern between the contact resistances at the interfaces in the thin film stack and series resistance in the bulk of the thin films. In the following, we therefore use a lumped value, which we label contact resistance, ρ_c, for the sake of simplicity.

At the front side, the MgO/c-Si and MgO/i-aSi:H/c-Si layer stacks with different thicknesses of MgO layers were realized. As it was shown before, the passivation of the c-Si substrate by such layer stacks can be improved by a short annealing step at 200-250 °C. Therefore, before the metallization was applied, samples were annealed at 250 °C for 5 minutes. Afterwards, 2 µm thick circular aluminum pads of different sizes were evaporated onto the front side. For both cases, i.e. with and without i-a-Si:H buffer layers, J(V) characteristics had a linear, Ohmic behaviour as shown in fig. 5. It is possible to see that with increasing MgO layer thickness there is a drastic increase of resistance, by four orders of magnitude and scaling roughly exponentially with ALD cycles, i.e. with layer thickness. The conduction band offset between MgO layer and c-Si is around 1.55 eV[36]. The band offset between c-Si and i-aSi:H is around 0.2-0.3 eV[37]. By assuming transitivity rule[38], the conduction band offset between MgO and i-aSi:H is still around 1.25-1.35 eV. With such a high barrier higher than thermal energy k_bT. Thus, tunneling of electrons from the a-Si conduction band through the MgO to the metal contact is probably the main current transport mechanism, and an exponential scaling of resistance with barrier thickness is consistent with this argument. Therefore, this increase can correspond to the domination of tunneling resistance[39]. With the increase of the layers thickness, J(V) data becomes more scattered. Therefore, the contact resistivity for thicker layers could not be reliably determined from the thicker layers. As a result, in the following we only discuss data obtained from the test structures with 30 ALD cycles of MgO, for both cases i.e. with and without i-aSi:H. For the MgO/c-Si stack the contact resistance of the structure is 0.18±0.01 Ωcm^2, which is comparable with estimates obtained by others for evaporated MgO layers for similar layer thickness[12]. In the case of the i-aSi:H, the extracted contact resistance is about five times higher: 0.95±0.11 Ωcm^2. Inserting of i-aSi:H by itself introduces an additional resistance to the

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current transport though the contact system,

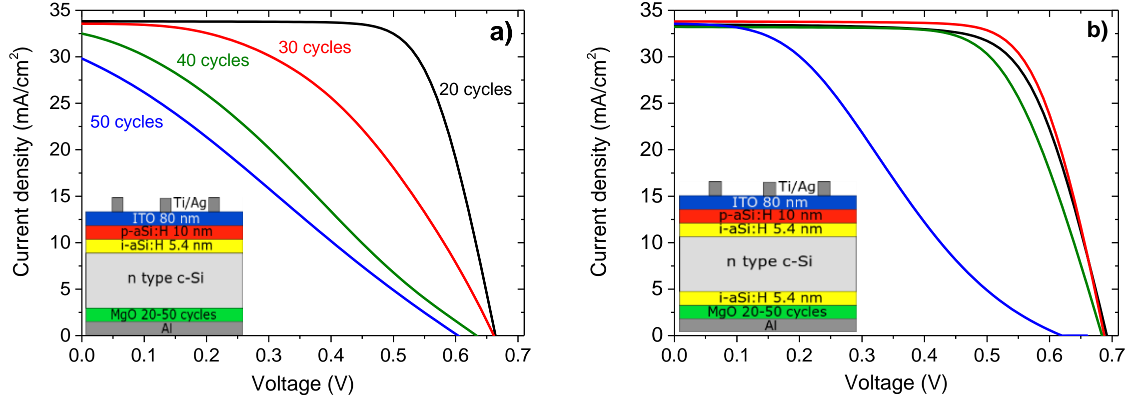

Fig. 6. Illuminated one-sun J(V) characteristics for solar cell devices with a) an MgO/c-Si layer stack as electron contact on the rear side, b) an MgO/i-aSi:H/c-Si stack. The MgO layer thickness was varied. Colors of the curves for both graphs represent the same number of deposition cycles. Schematic representations of the devices are shown as insets

due to the bulk resistivity of this undoped layer[40]. Additionally, one of the possible reasons for such an increase can be due to the aluminum metallization: the Al contact is shown to be suitable in combination with MgO material[12]. However, in the case of very thin layer of MgO, there is a possibility that aluminum diffuses through the layer to the i-aSi:H interface. . The interaction of Al with the a-Si:H.

F. MgO layers as electron contacts in silicon heterojunction solar cells

TABLE I. SOLAR CELL PARAMETERS FOR THE BEST DEVICES FABRICATED ON PLANAR SI WAFER INCORPORATING THE ALD-GROWN MGO LAYERS.

Sample type	*MgO cycles*	*Jsc (mA/cm2)*	*Voc (V)*	*FF (%)*	*Efficiency (%)*
MgO/c-Si	20	33.4	0.664	73.8	16.4
MgO/i-aSi:H	30	33.8	0.687	72.4	16.8
Reference	0	33.3	0.698	73.4	17.0

Finally, solar cells with MgO/c-Si and MgO/i-aSi:H/c-Si layer stacks as rear contacts were fabricated.

The MgO layer thickness was varied in the range of 20-50 ALD cycles to see the influence of the layer thickness on the final solar cell performance. In Fig. 6 the J(V) characteristics for such devices are shown. Additionally, Table 1 shows the J(V) parameters of the best cell for each type of stack. Note, that due to the flat surfaces of the c-Si wafers used for these cells, the short circuit current is strongly limited. For cells with the MgO/c-Si stack, an efficiency of 16.4 % is achieved with a thin MgO (20 ALD cycles, $d_{MgO} \approx 2.5$ nm). For comparison, a reference cell with an (n,i)-a-Si:H contact reaches and efficiency of 17%. With a further increase in layer thickness, we observe that a transport barrier is formed, which is reflected in the S-shape of J(V) curves and a decrease of V_{oc} and FF. This degradation is in line with the increasing contact resistance that was discussed earlier. For the layer leads to counterdoping [41], yielding an increase of the total contact resistance [42]. Note, that the contact resistance obtained for the reference stack for the SHJ solar cell (c-Si/i-aSi:H/n-aSi:H/ITO/Ti-Ag) is even higher, estimated to 1.1±0.15 Ωcm^2 in comparison to regarded stack.

MgO/i-aSi:H/c-Si stack, it is obvious that the additional thin i-aSi:H layer helped to keep the passivation on a level that allows V_{oc} values above 680 mV. Improved passivation allowed to have the higher FF for thicker MgO layers. This shows that the i-aSi:H layer makes it possible to sustain the passivation, and that a thin layer of MgO is sufficient to function as a proper electron transport layer. The slight degradation of the V_{oc} and FF for such stacks as compared to the reference can be attributed to the possible diffusion of aluminum through the MgO stack during the evaporation of the aluminum contact. In addition, the FF is probably decreased by the additional series resistance in the (i)a-Si:H film.

IV. CONCLUSIONS

We have presented an investigation of low temperature ALD of magnesium oxide layers on

c-Si(n) and i-aSi:H/c-Si(n) substrates, at deposition temperatures of 125-200 °C. We investigated the interface passivation and layer properties of these layers, as well as the behavior of such layers upon an additional annealing step.

A weak passivation effect yielding minority carrier lifetimes of 0.15 ms was observed for a ~9.8 nm thick MgO layer directly deposited on c-Si after an annealing step of 200-250 °C. For the alternative layer stack of MgO/i-aSi:H on c-Si, after the initial MgO layer deposition, we observe a degradation of minority charge carrier lifetime caused by an increase of recombination-active

defects either at the MgO/i-aSi:H interface or in the MgO bulk. Upon a short annealing step of 5 minutes at 200-250 °C, it was possible to not only fully recover the passivation, but also gain a further improvement. The main reason for this improvement can be explained from XPS measurements: The as-grown MgO layer is not fully stoichiometric, and Mg(OH) moieties are present, as evidenced by the corresponding contributions to the Mg 2p and O 1s core levels. Upon annealing, the layers become more stoichiometric, thus less defective. Furthermore, the released hydrogen probably diffuses to the i-aSi:H/c-Si interface and causes the passivation improvement of the stack.

Additionally, we observed that for both types of layer stacks the contact showed an Ohmic behavior. However, with the increase of MgO layer thickness, the contact resistance increased drastically. For the device relevant MgO thicknesses of around 3 nm (30 ALD cycles), the contact resistance in the MgO/c-Si layer stack was approximately 0.18 Ωcm^2, and for the MgO/i-aSi:H/c-Si stack 0.95 Ωcm^2. Thus, for both contact stacks, there is a tradeoff between the passivation quality and the contact resistance. As a proof of concept, silicon heterojunction solar cells with both types of the layer stacks used as electron selective contacts and standard (p,i)a-Si:H hole selective contacts were fabricated on flat wafers. The cells show similar power conversion efficiencies of above 16.4 % for both cases. Therefore, we conclude that our ALD MgO layers can be considered as a suitable building block for further development in c-Si based devices. Furthermore, the low process temperatures < 200°C ensure compatibility with the well-established a-Si-H/c-Si heterojunction technology as used in high efficiency cells. Possible further routes for improvement include the optimization of the metal contact and the interface with the i-aSi:H layers. Also, the deposition of MgO on top of an intentionally ultrathin oxide rather than an HF-last Si surface can be considered as a route to achieve improved contact properties and passivation.

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