$CuGaSe_2$ / c-Si Tandem solar cell exceeding 1 Volt V_{OC} with passivating tunnel junction

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Outline

Introduction & Context

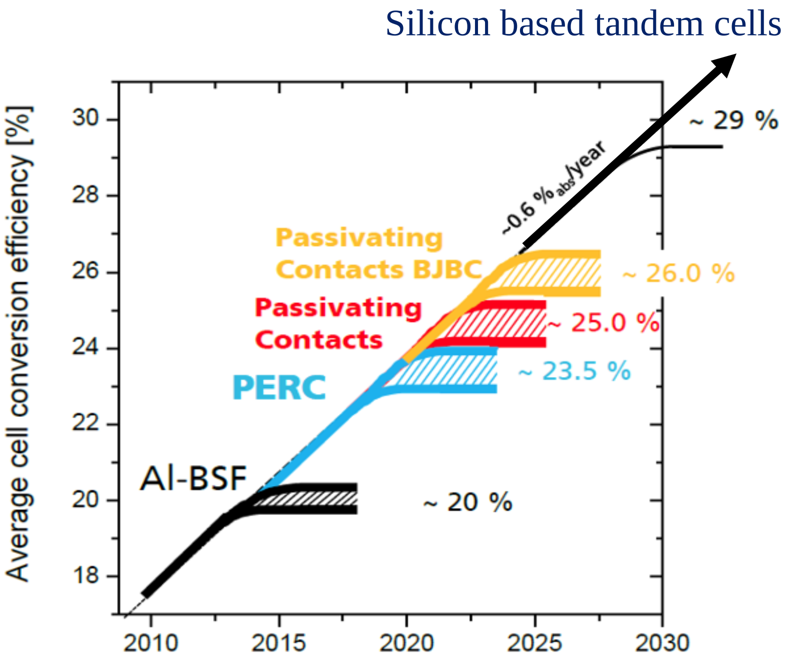
$CuGaSe_2$ (CGSe) growth studies

$CuGaSe_2$ / c-Si tandem solar cell

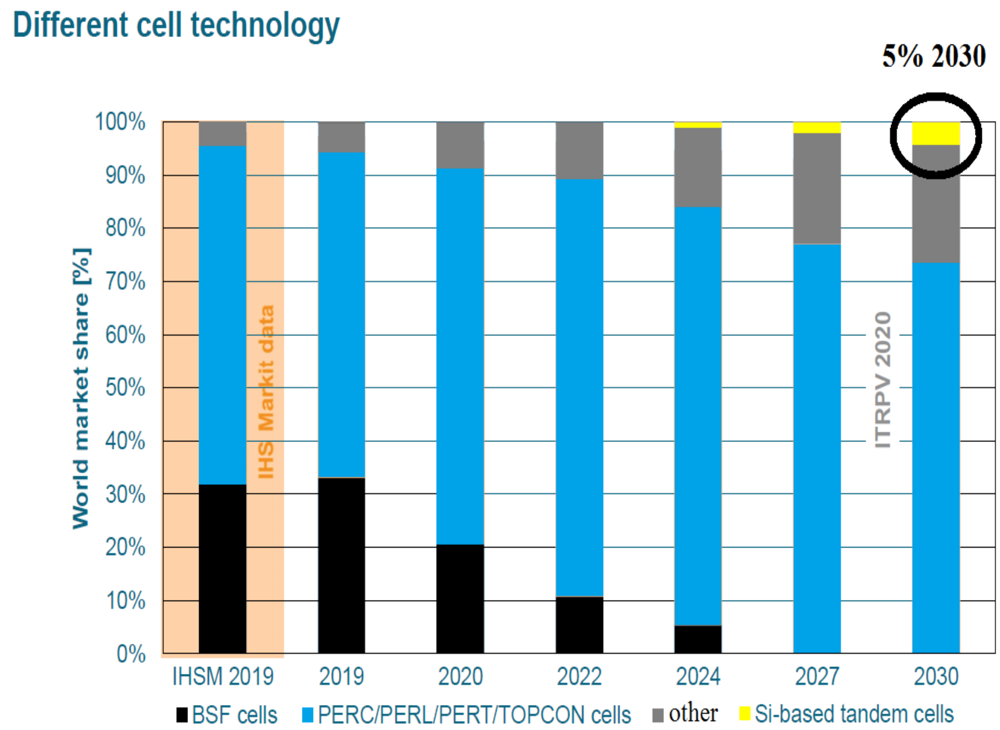
Conclusion

CONTEXT: toward a tandem industry

Conversion efficiency road map for c-Si based solar modules



Market share prediction for c-Si based solar modules

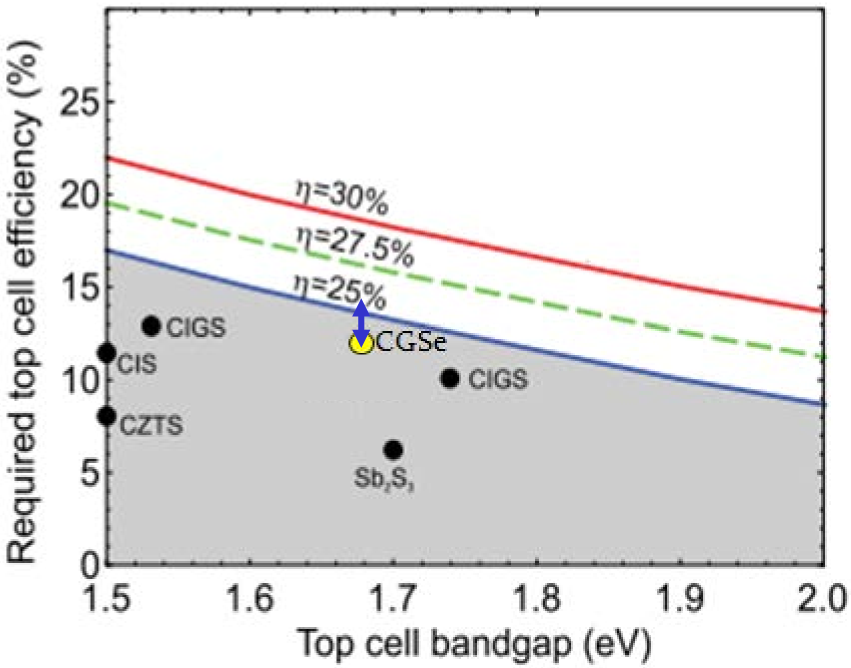


I. Gordon, presentation at Les Houches School of Physics, 2018
ITRPV, 2020

CONTEXT: CGSe close to be ideal

CGSe :

- **record efficiency = 11.9%[1] (Univ. Uppsala)**
- **top cell required efficiency (tandem >25%) = 13.5%[2]**



➡ Improve the CGSe crystaline quality

➡ Use a better candidate as buffer layer

➡ Optimize as top cell on silicon or TCO for 2-T tandem cell

[1] F. Larsson et al., Prog. Photovoltaics Res. Appl., 2017.
[2] T. P. White, N. Lal, K. Catchpole, IEEE J. Photovoltaics, 2014.

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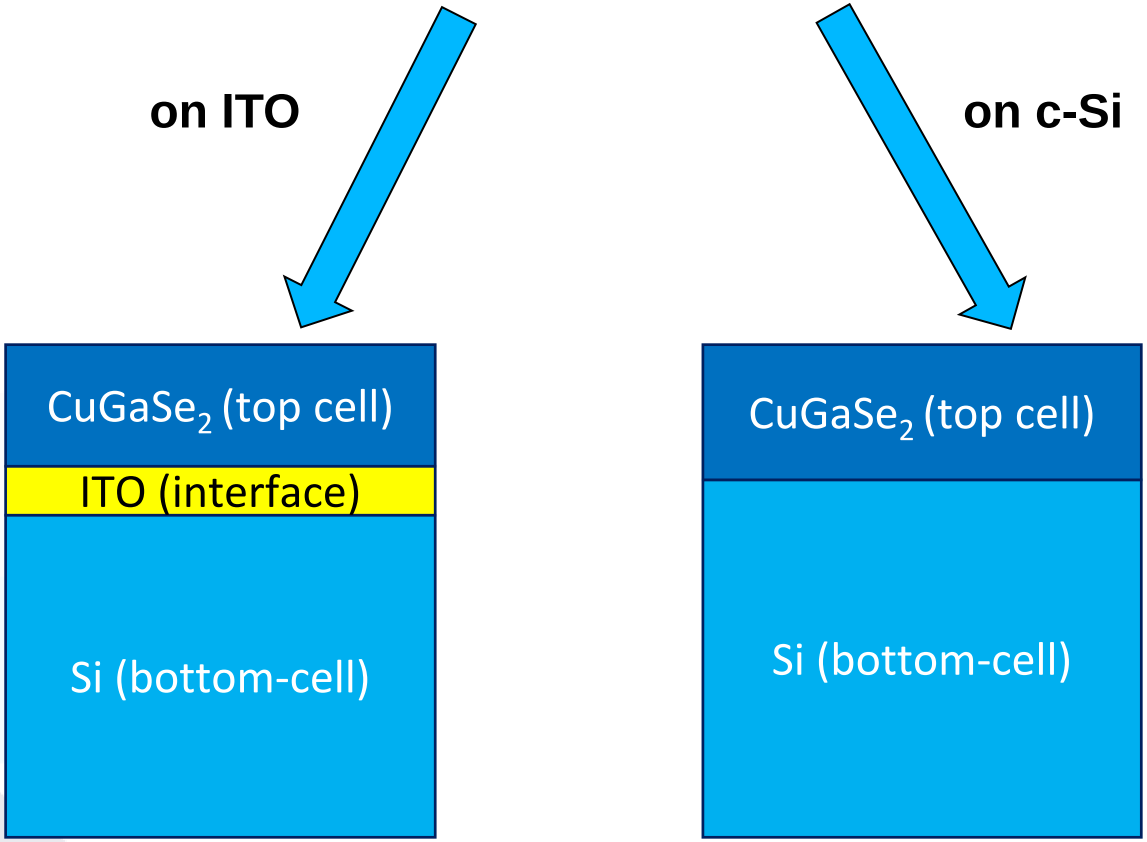
Top-cell: CGSe growth studies

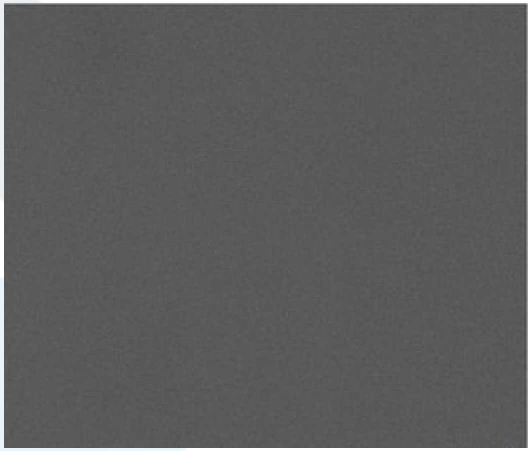
Deposition by co-evaporation

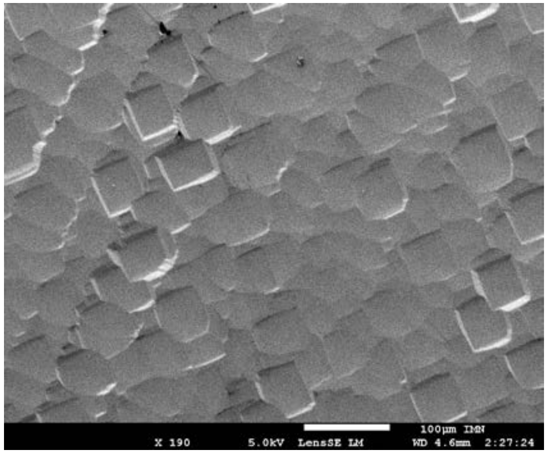


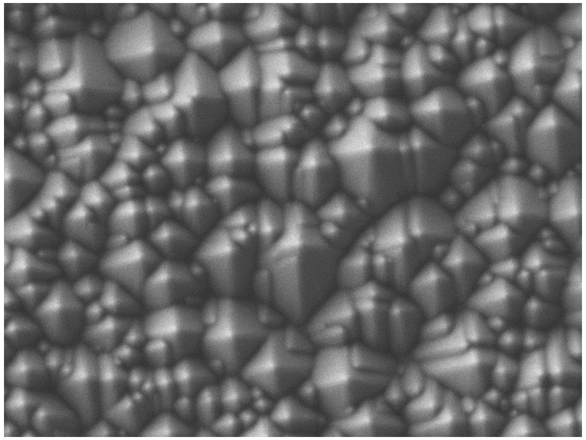
Deposition on c-Si
Surface roughness effects

CGSe thin film deposited on

Mirror-polished Si wafer	KOH-polished wafer	KOH-textured wafer

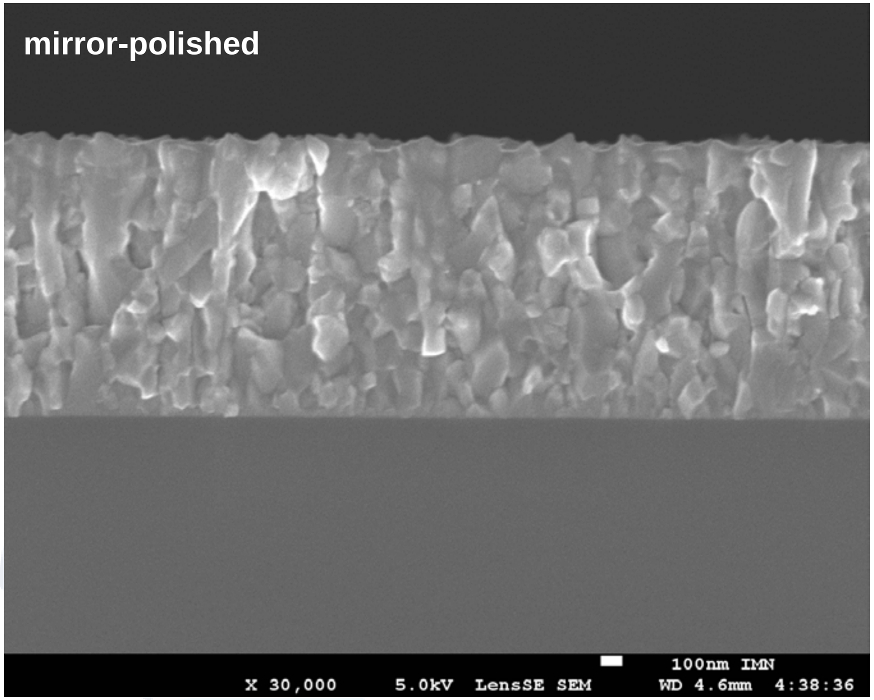


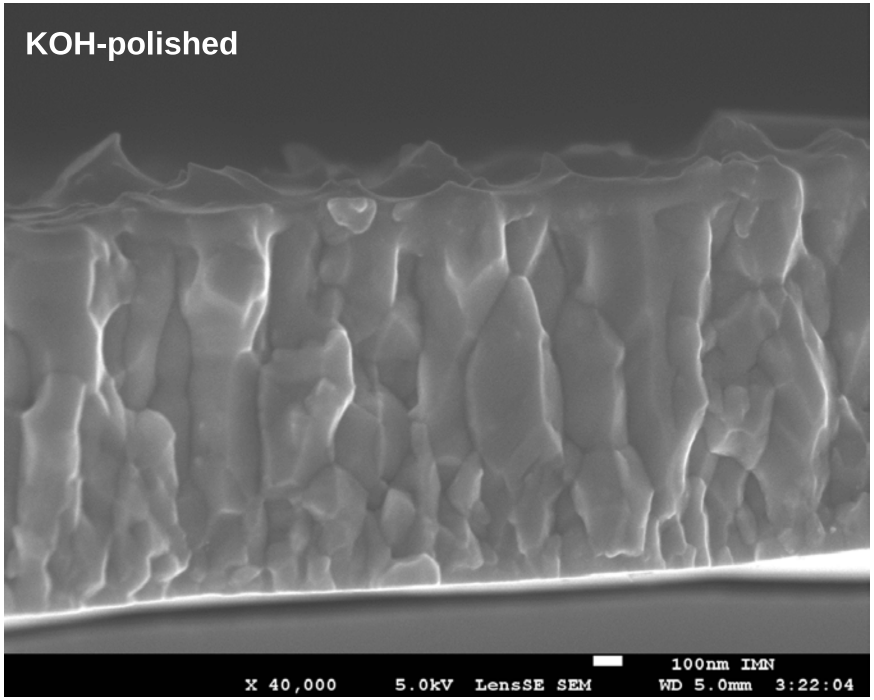




Analysis: SEM images

Surface roughness effects





KOH-polished wafer or mirror-polished wafer:

OBSERVATION: good morphology:
- no cracks,
- uniform thin film,
- large grains,
- good adhesion

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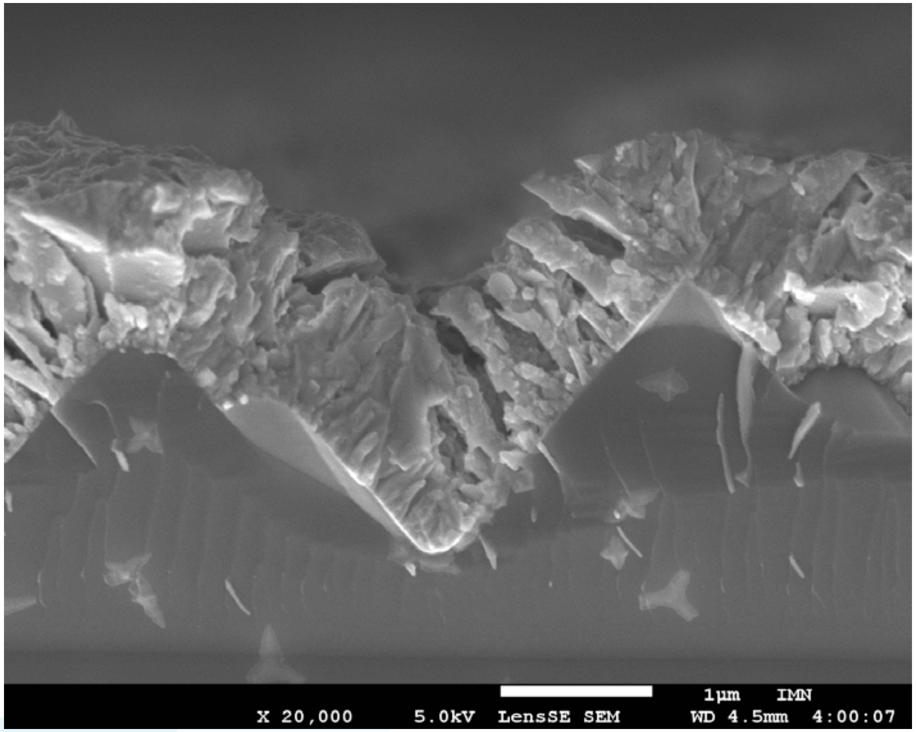
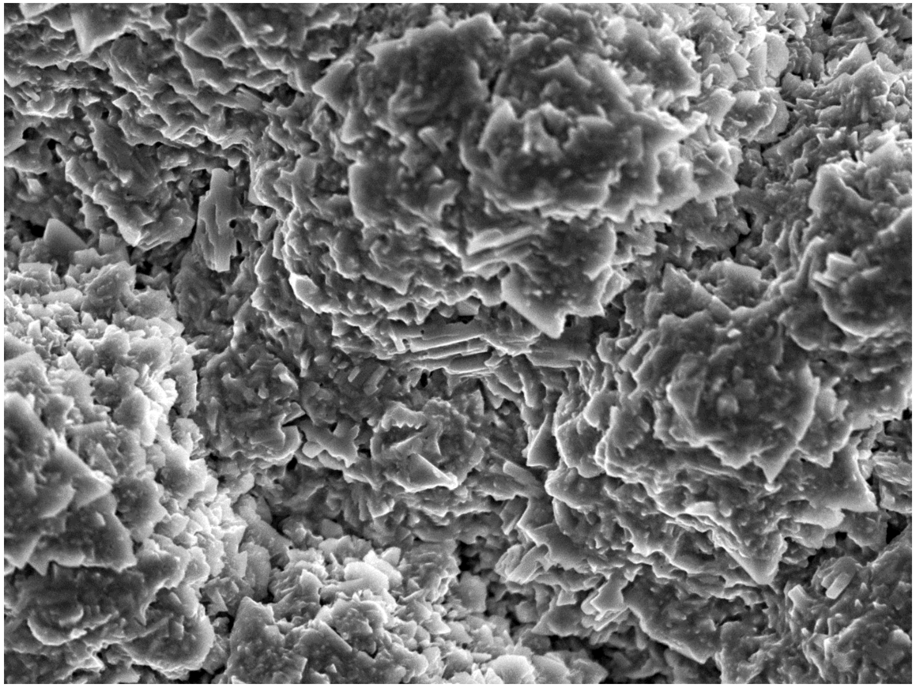
Surface roughness effects



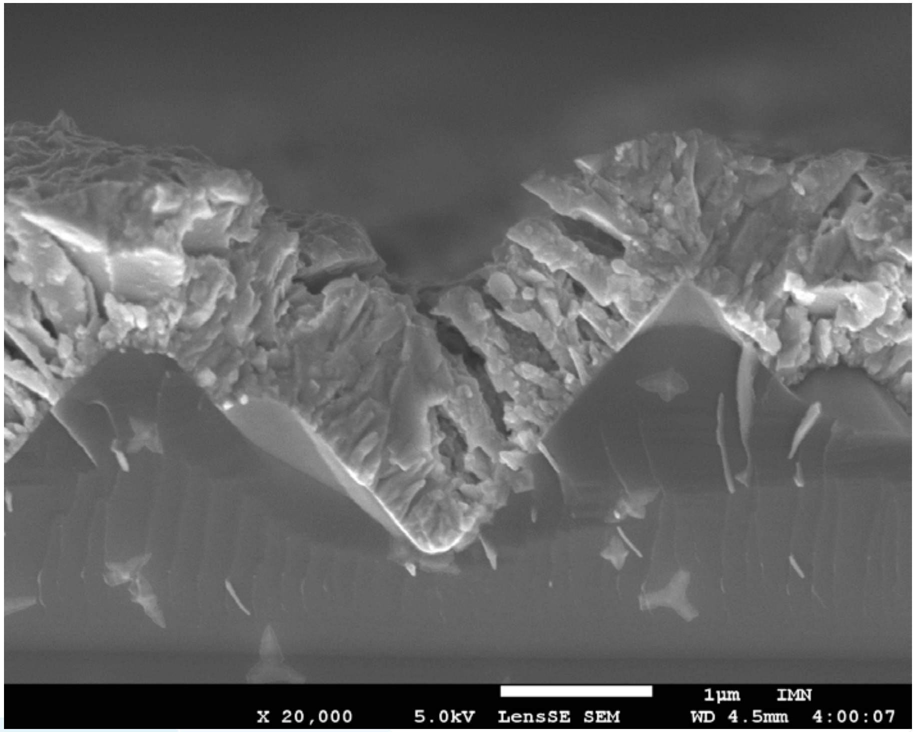


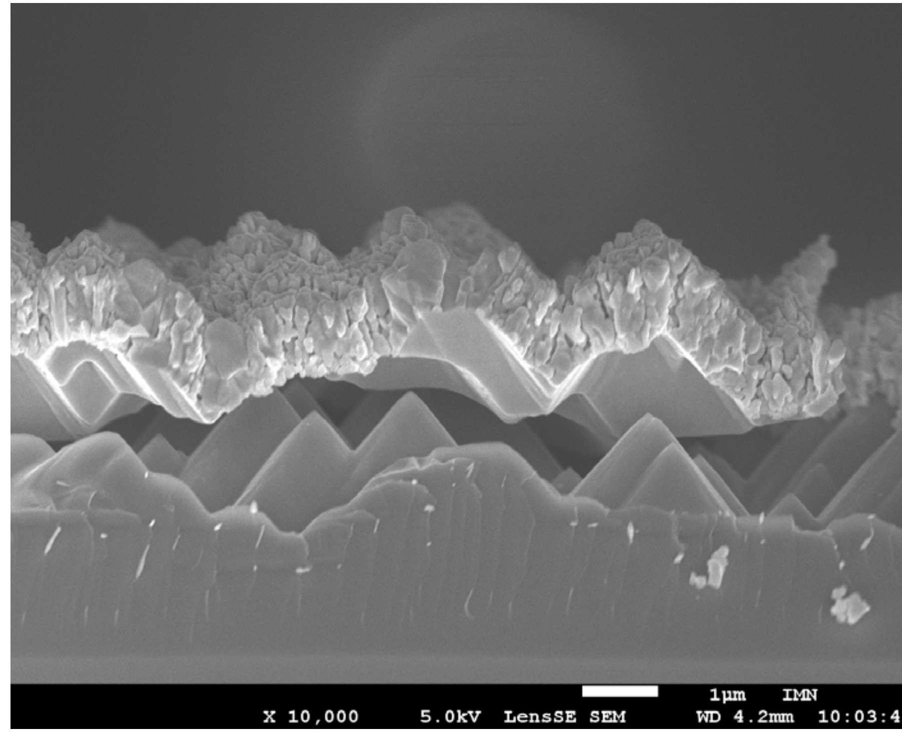
KOH-textured Silicon wafer

OBSERVATION:

- voids,
- non-uniformity
- small grains,
- poor adhesion

Surface roughness effects





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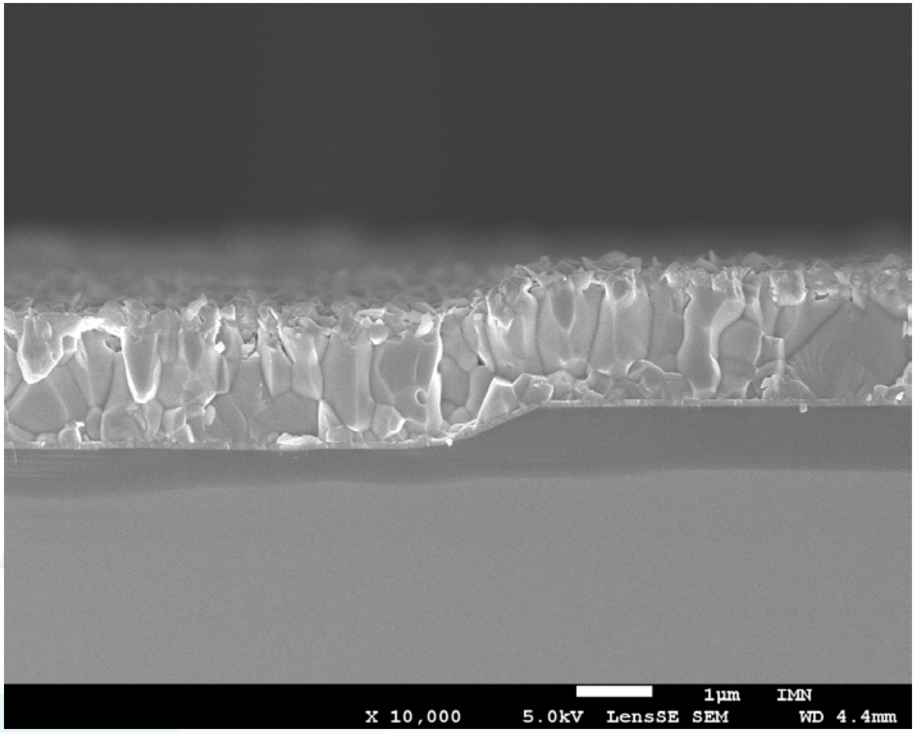
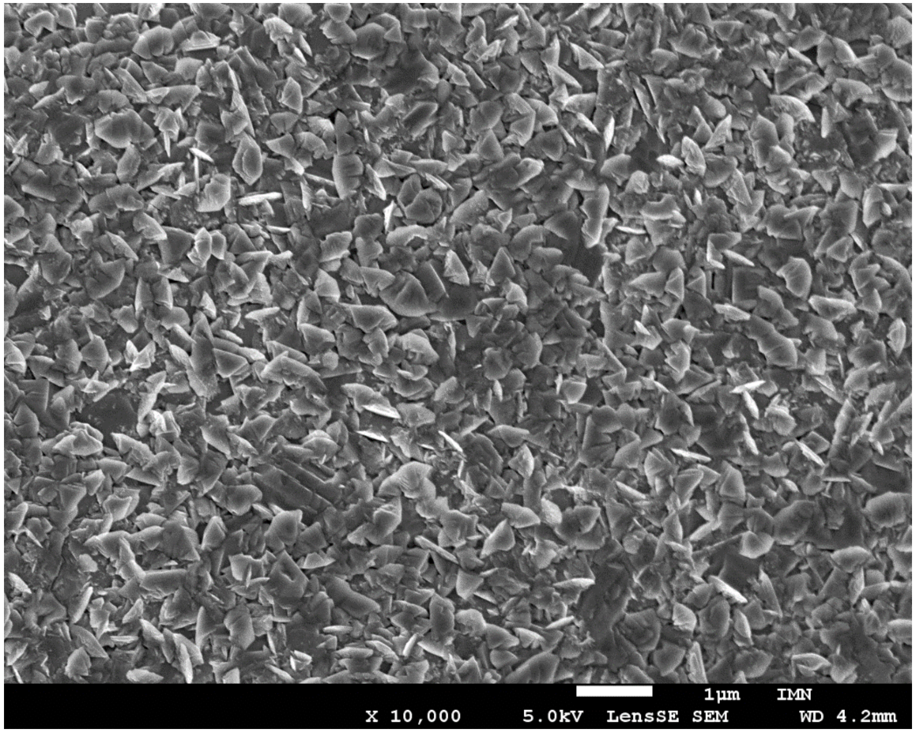
Deposition on c-Si / ITO





OBSERVATION: good morphology:
- no craks,
- uniform thin film,
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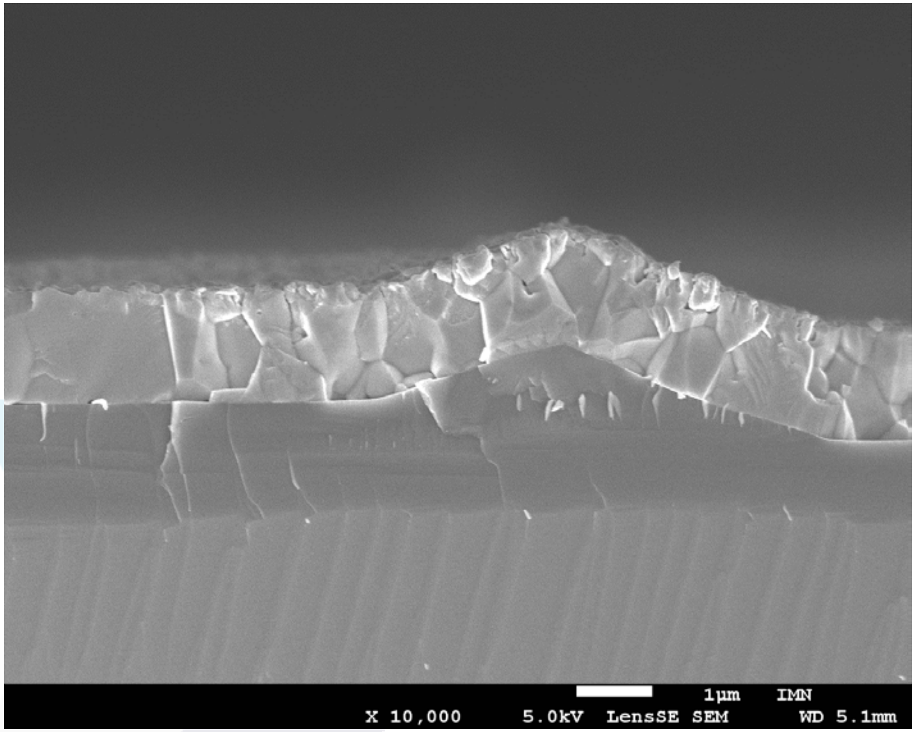
- no adhesion problem

Conclusions on growth condition

With KOH-polished Si wafer

CGSe on Si



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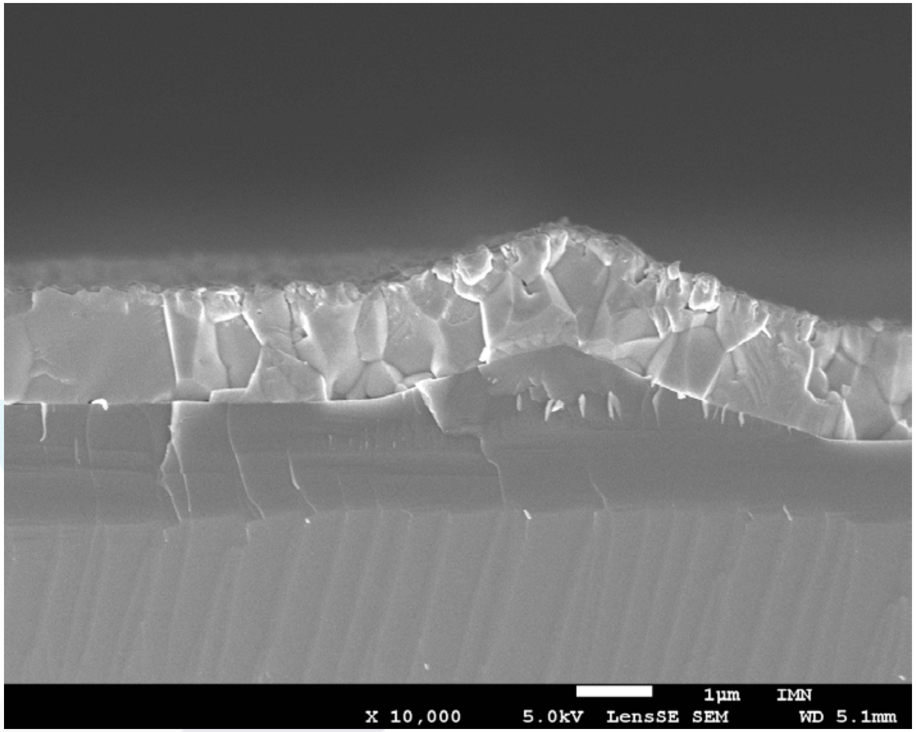
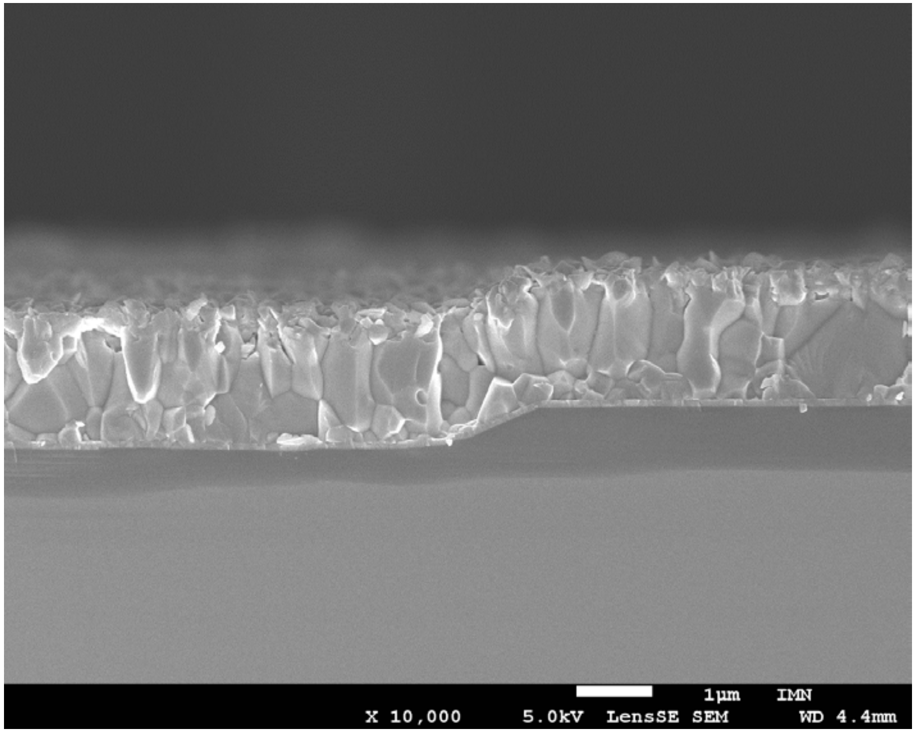


CGSe on Si / ITO



CGSe / c-Si tandem solar cell

Two possible routes

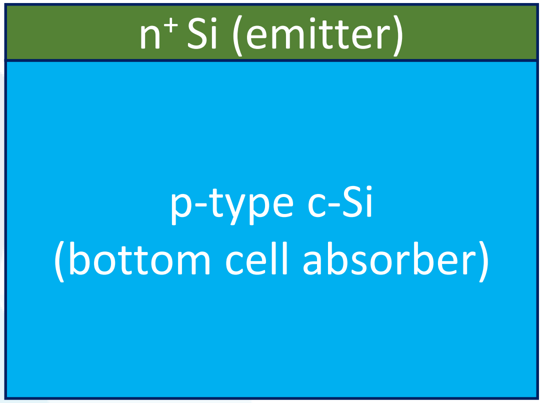
p-type c-Si
(bottom cell absorber)

ITO recombination layer

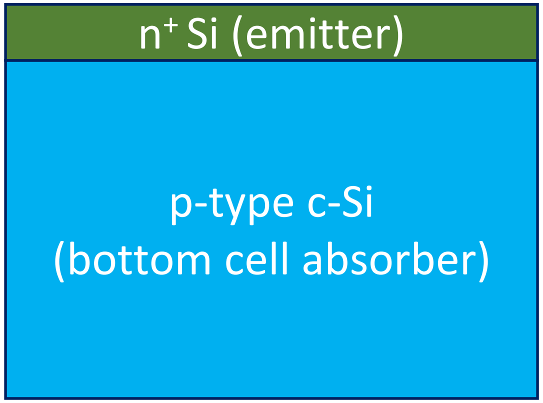
p-type c-Si
(bottom cell absorber)

Si Tunnel junction

Two possible routes



ITO recombination layer



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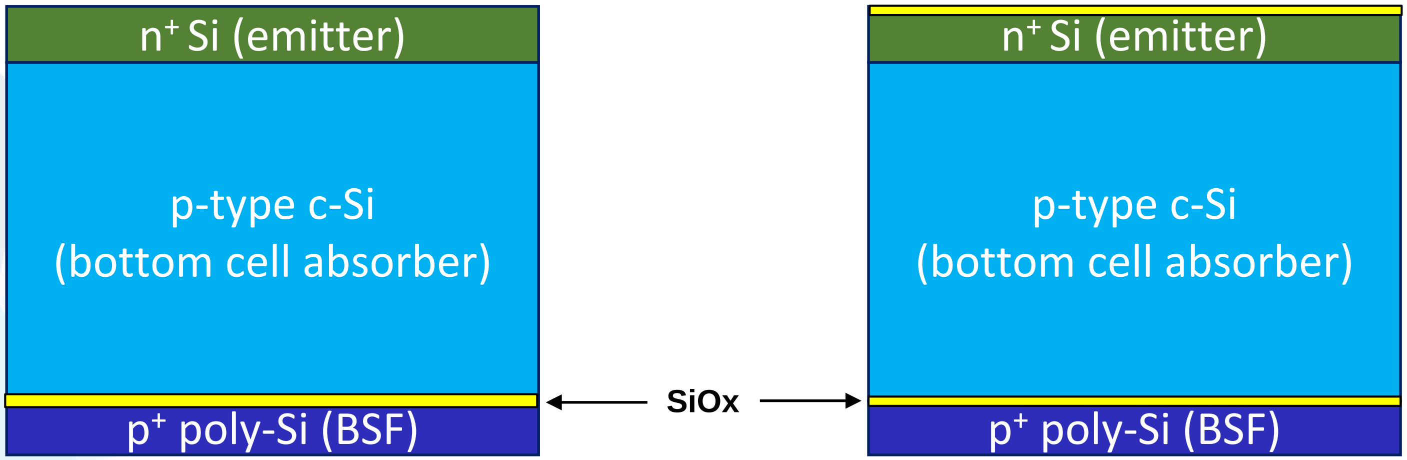

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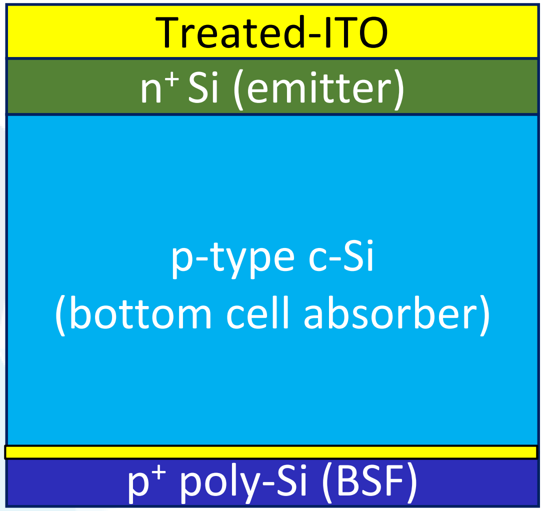

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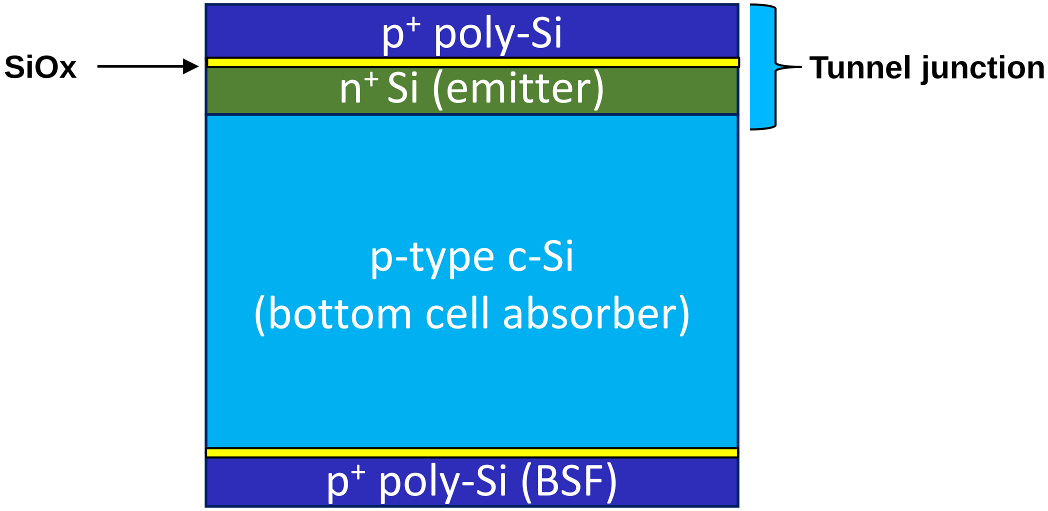

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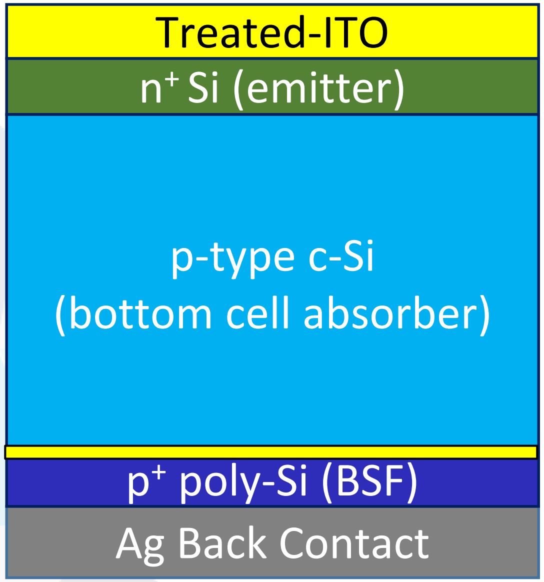

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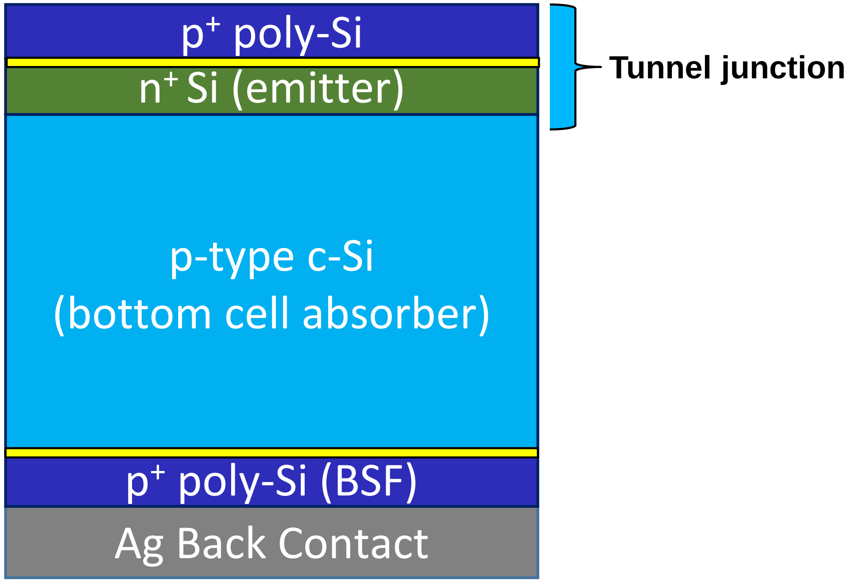

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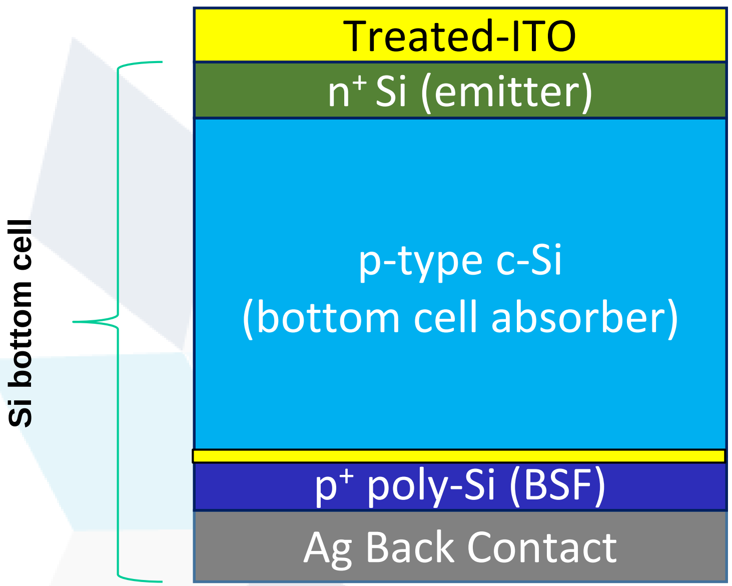

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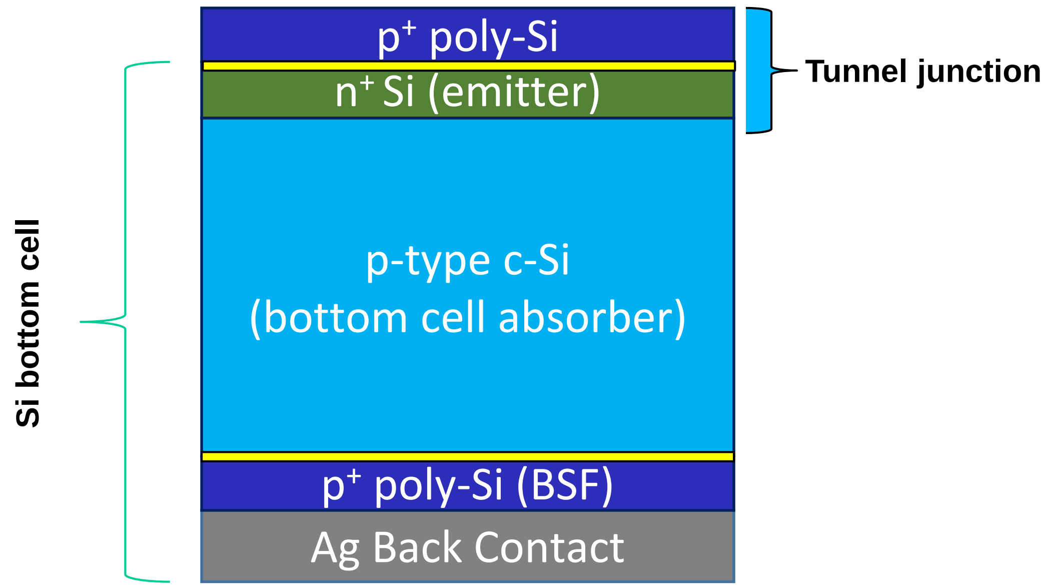

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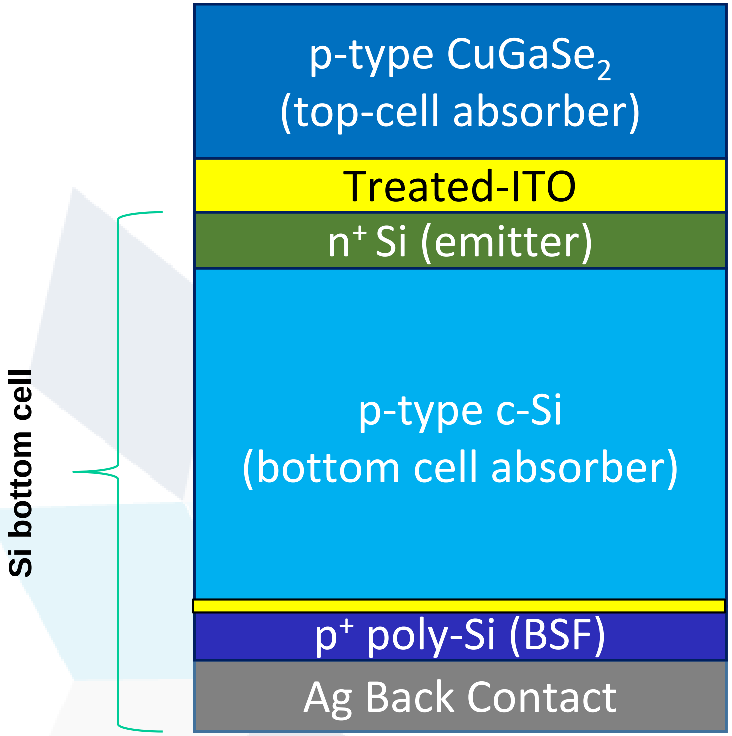

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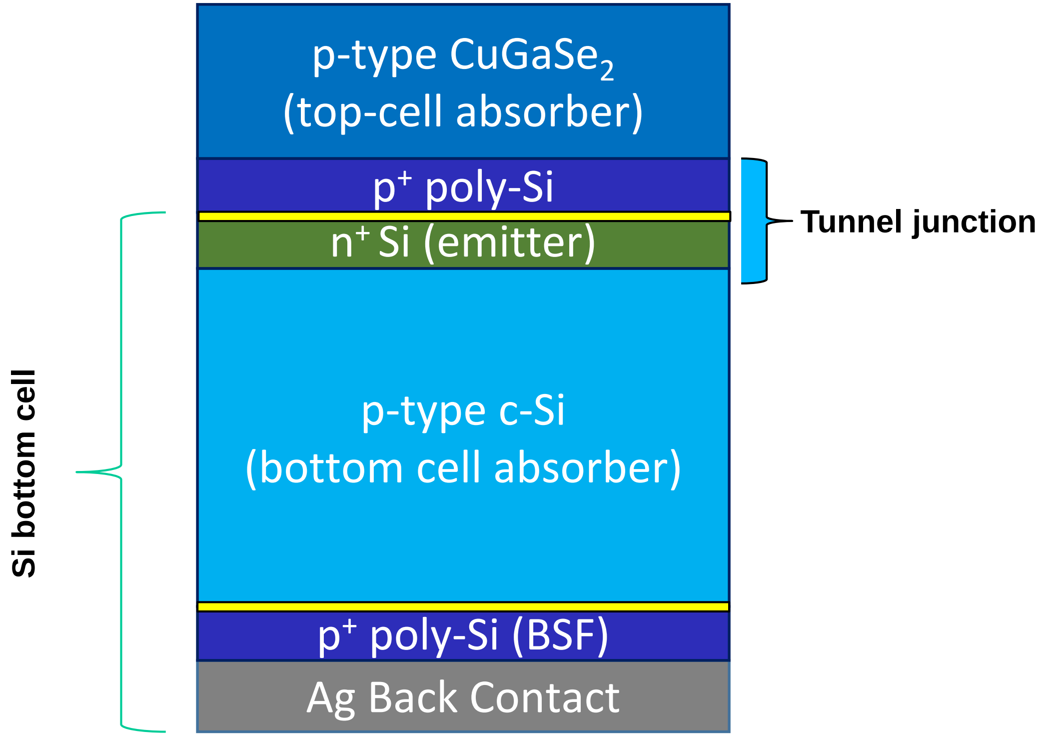

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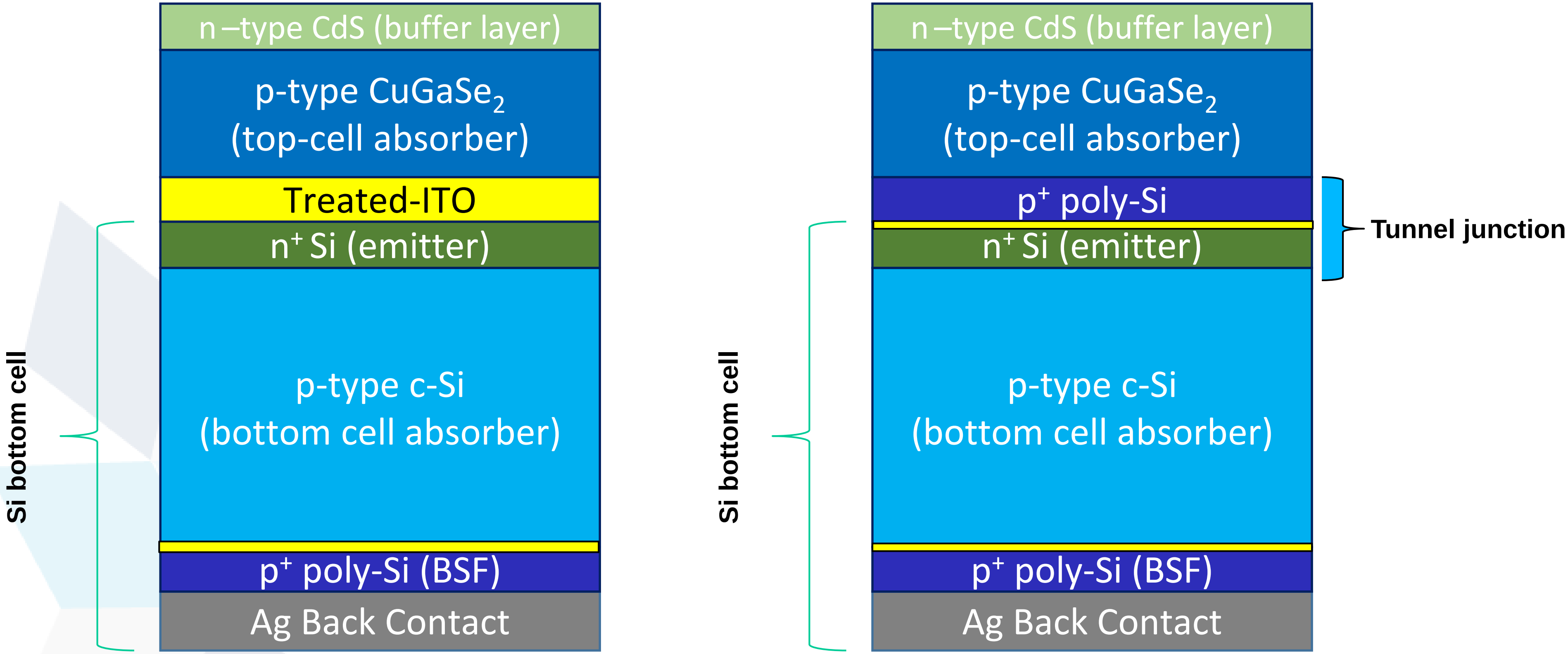

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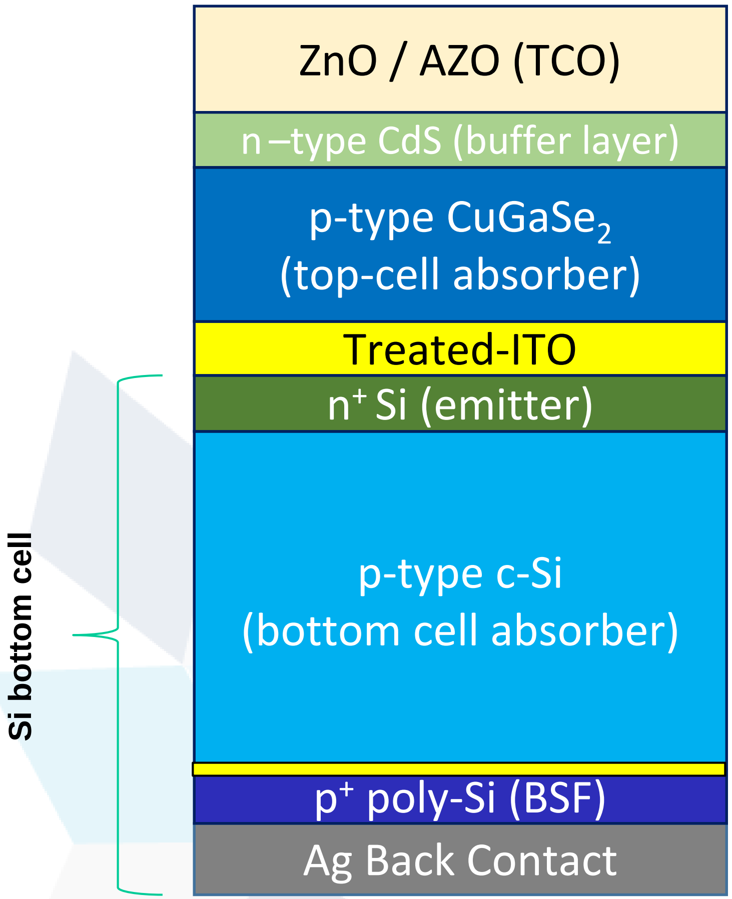

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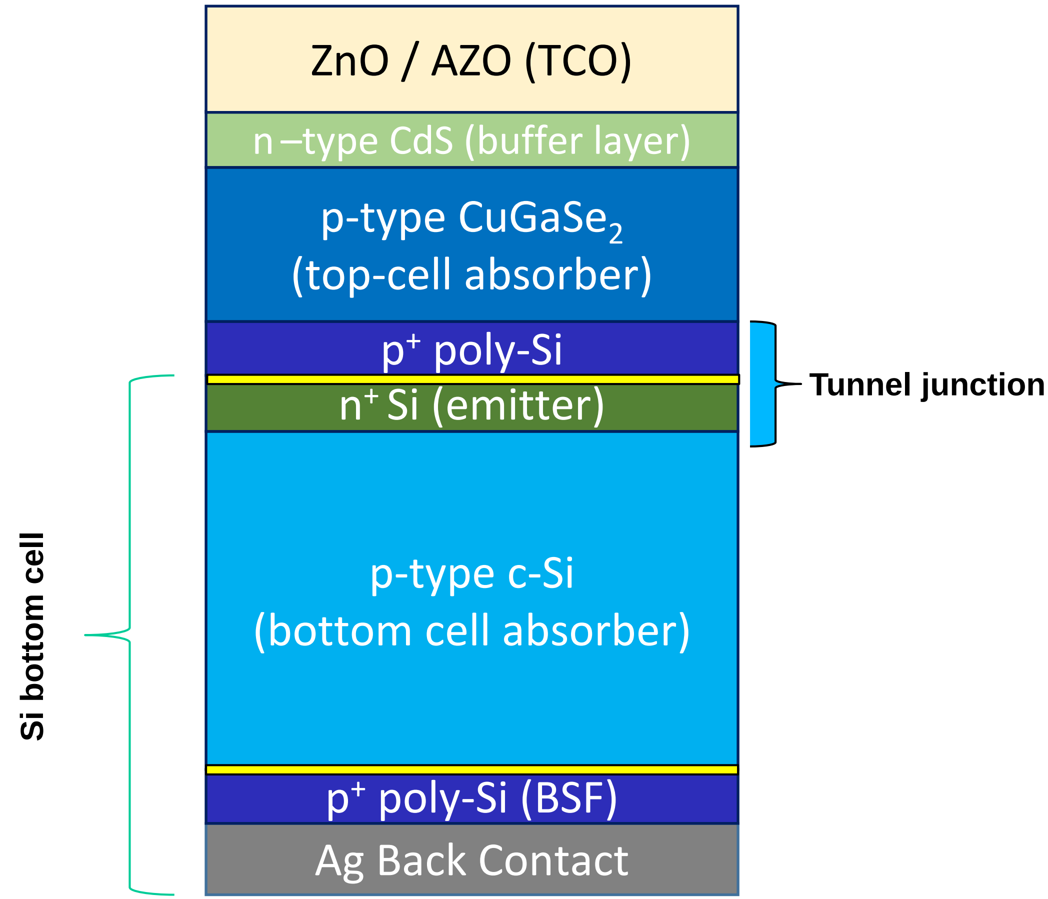

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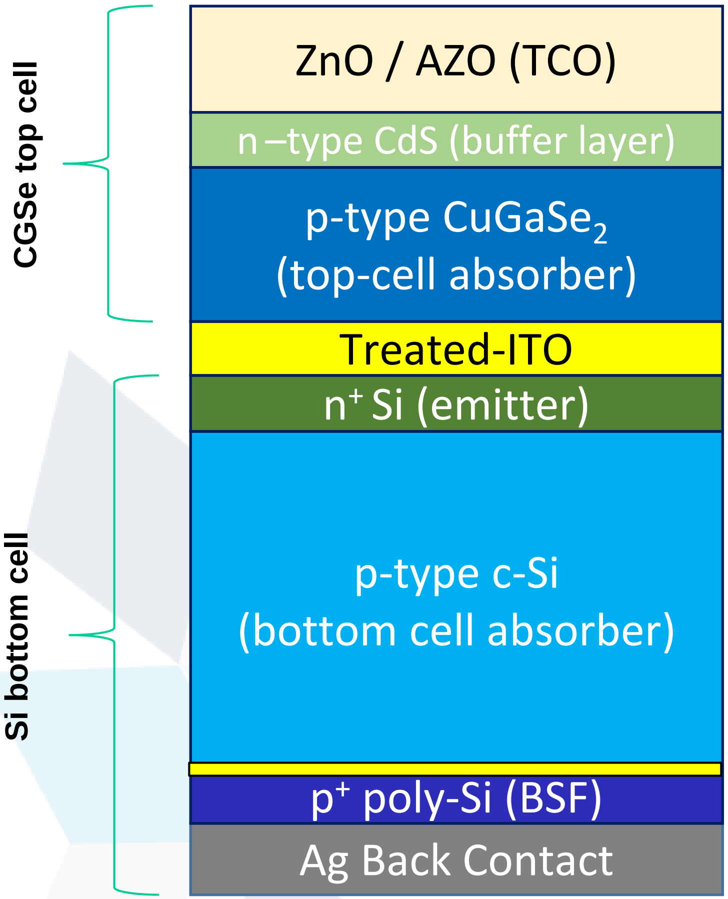

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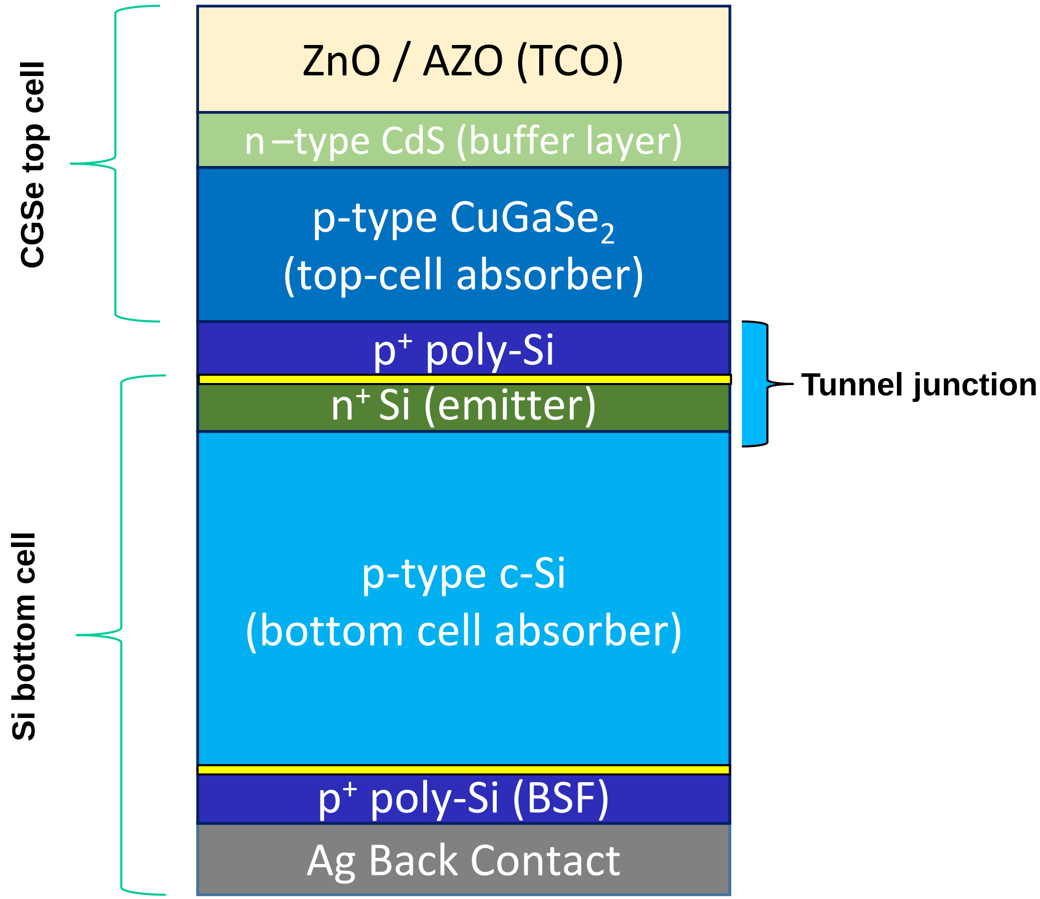
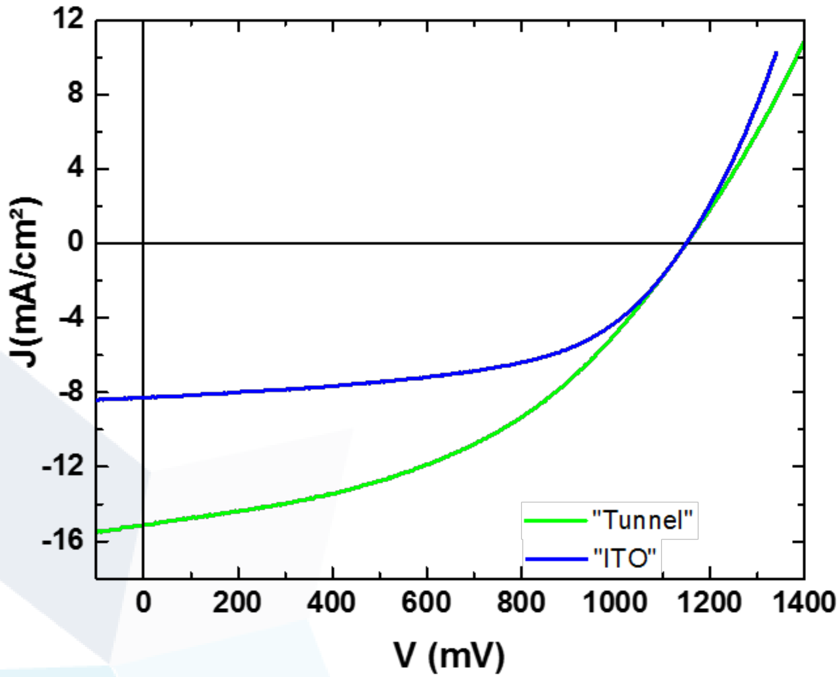


Si Tunnel junction

Results



Higher J_{SC} and efficiency with **tunnel junction**

	V_{OC} (V)	J_{SC} (mA/cm²)	FF (%)	Eff. (%)
ITO	1.15	8.0	56.5	**5.2**
tunnel	1.15	15.1	43.7	**7.6**

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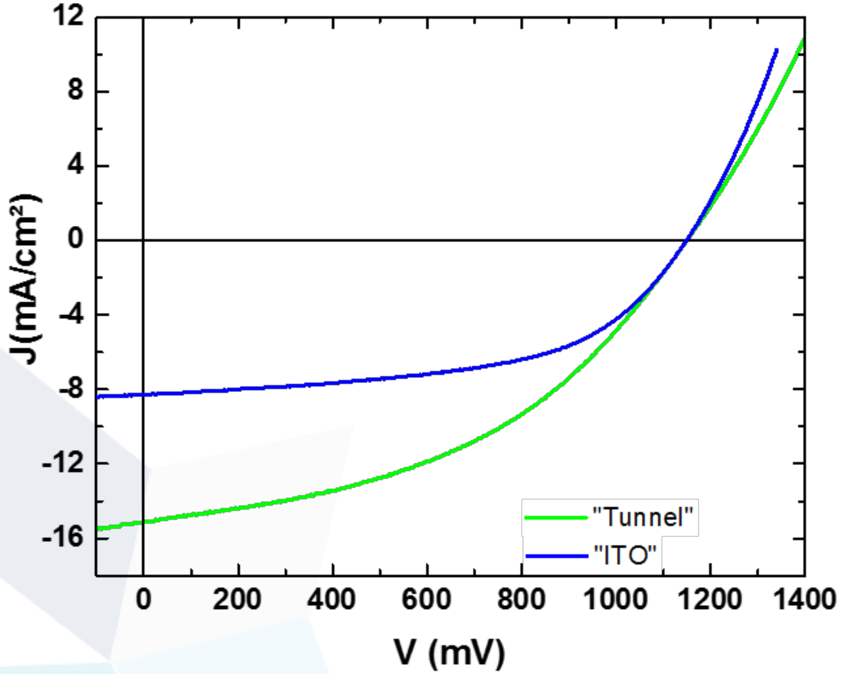

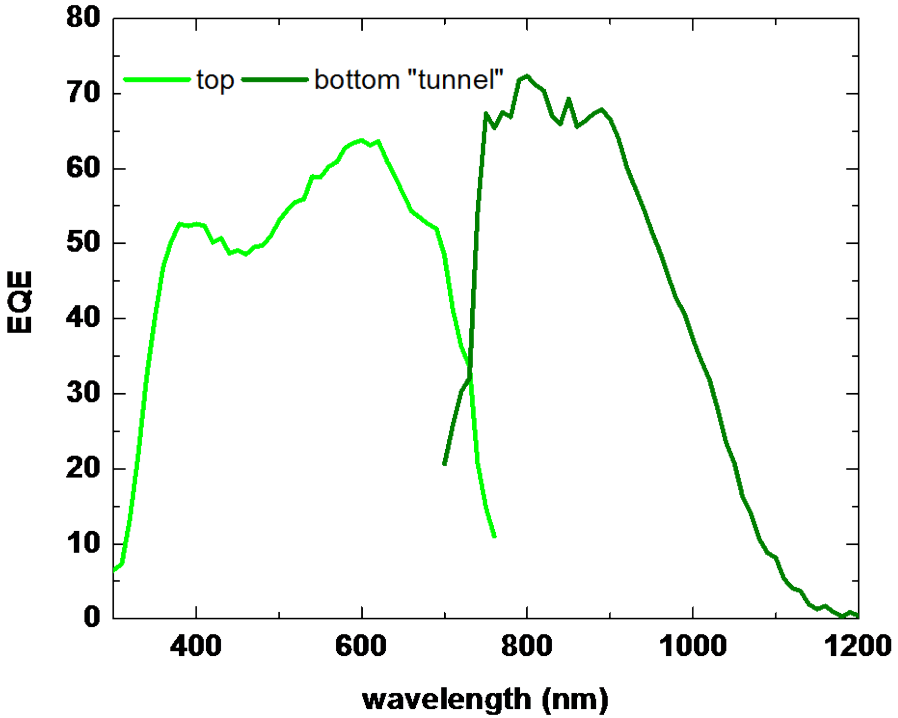

Higher J_{SC} and efficiency with tunnel junction

« ITO » Top cell back contact : **lower carrier collect**

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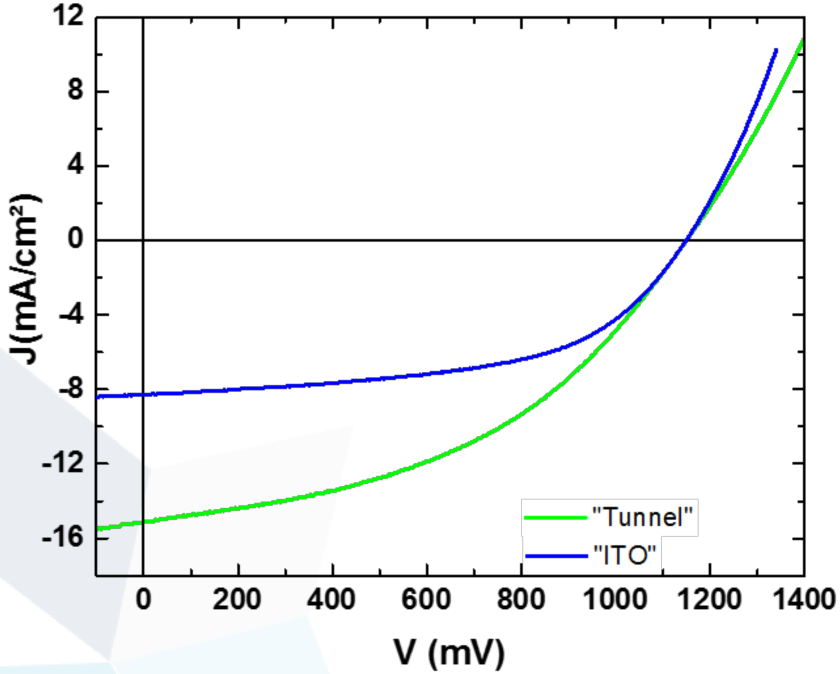

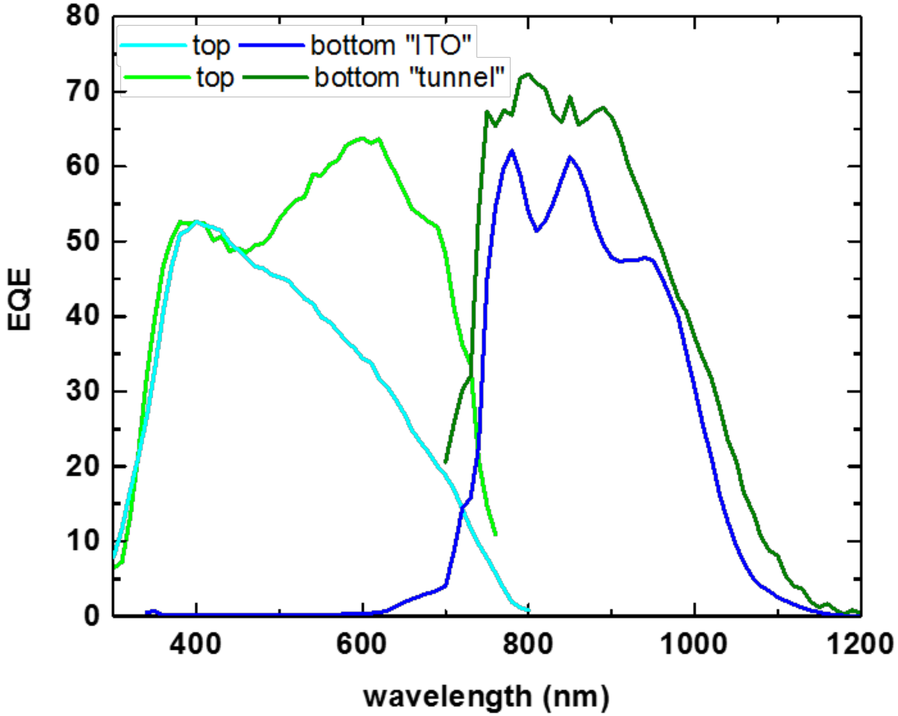

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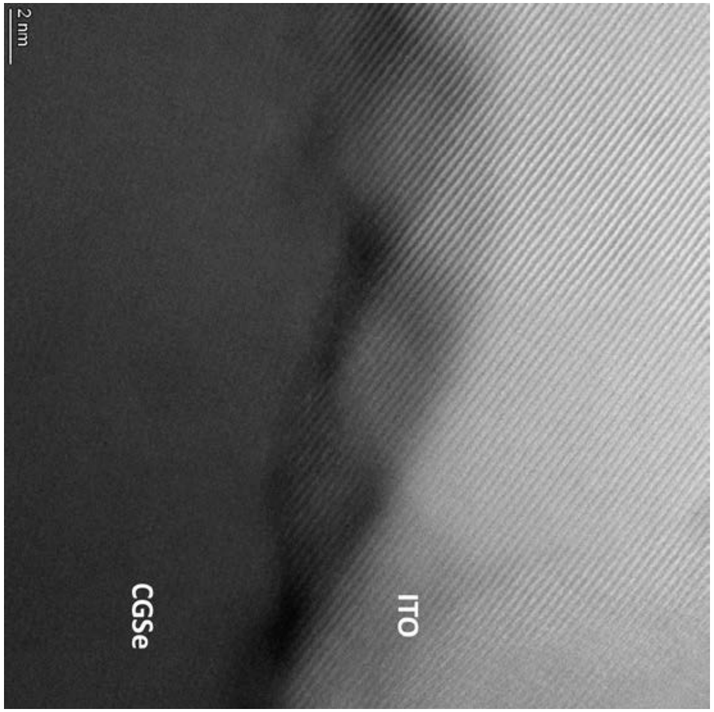
TEM analysis ITO / CGSe interface



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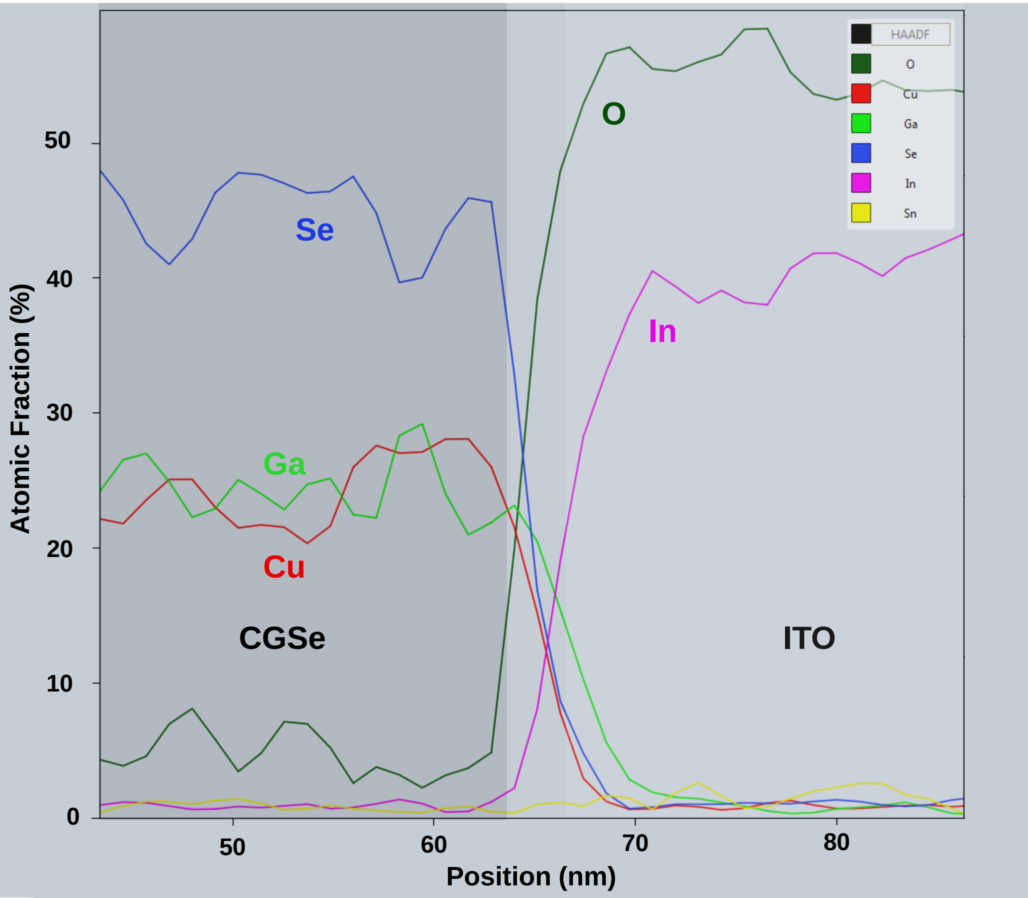

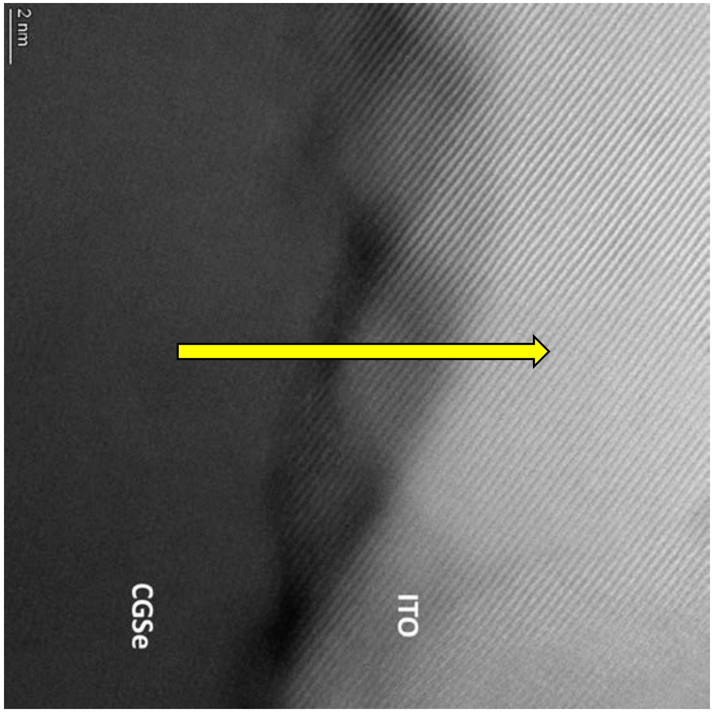

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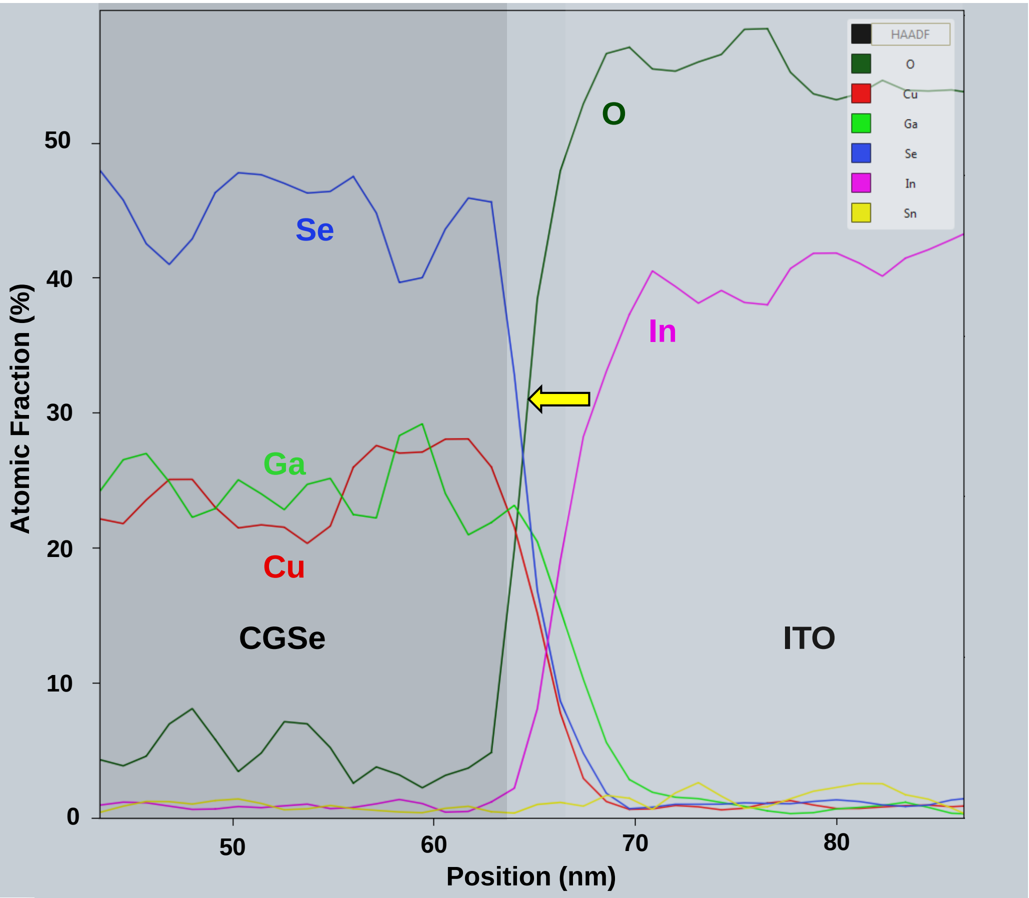

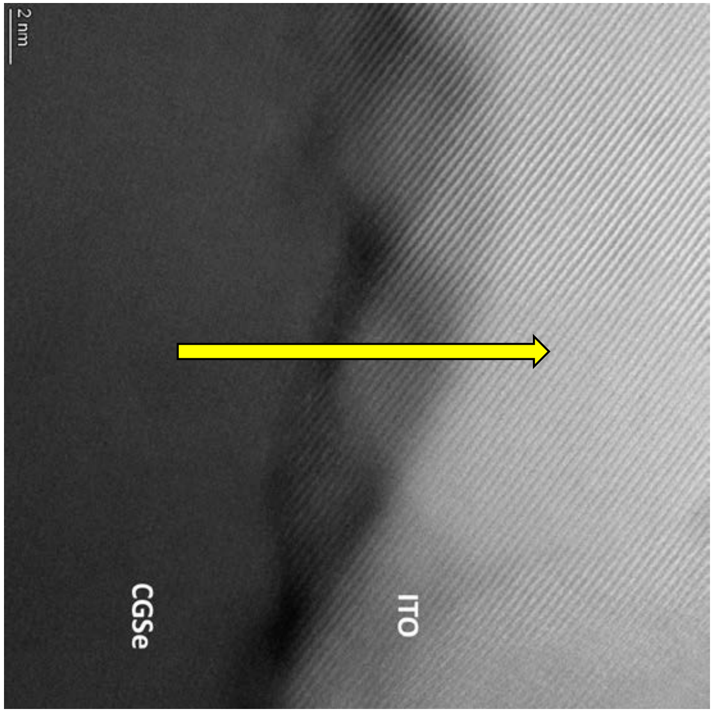

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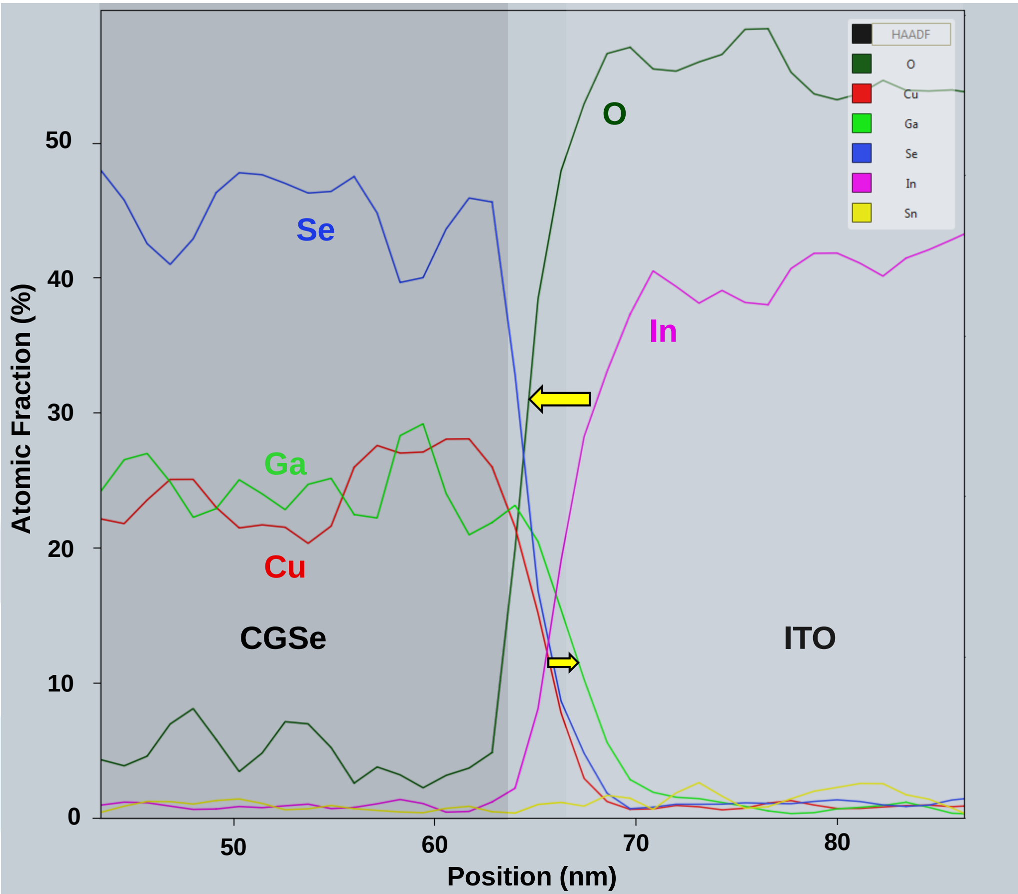

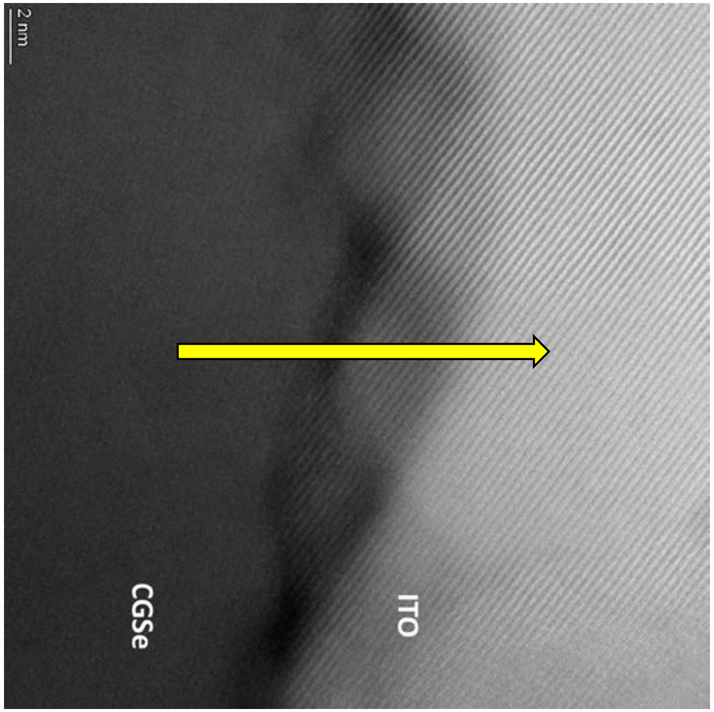

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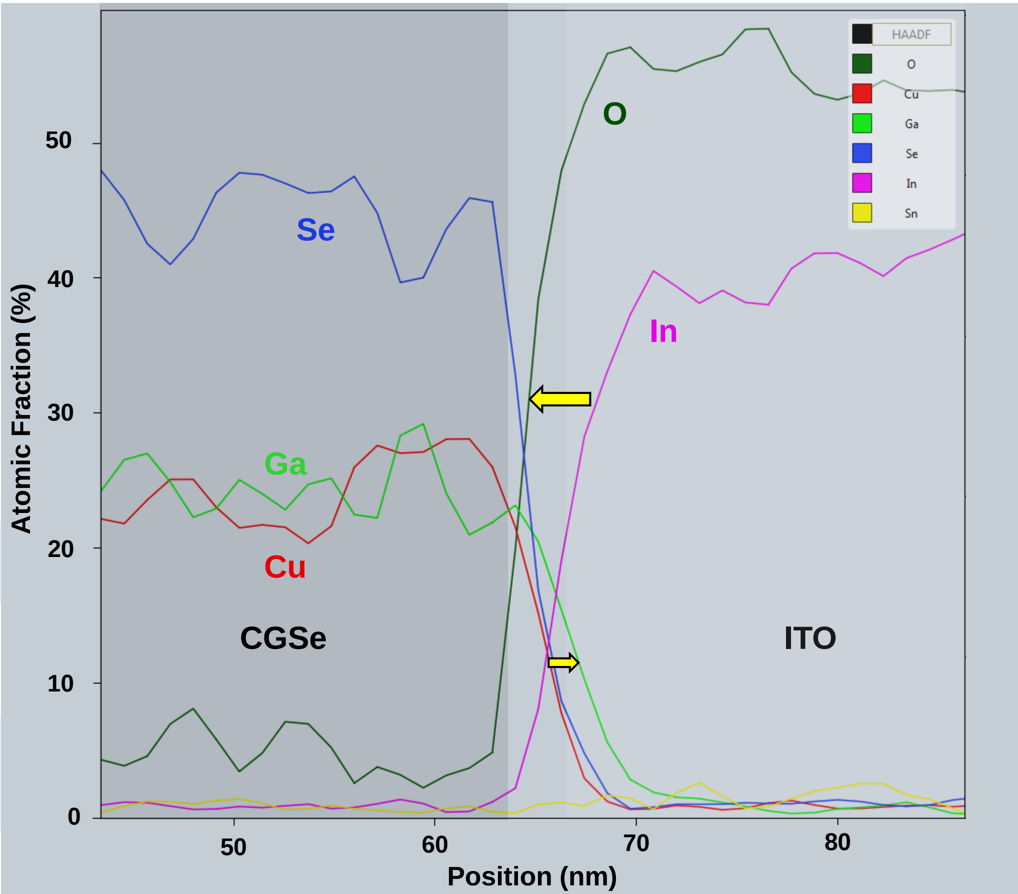
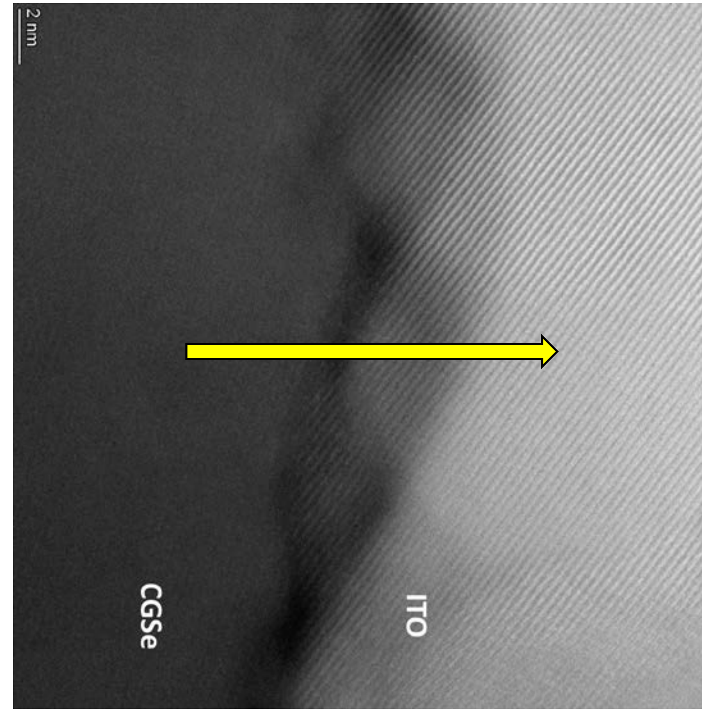
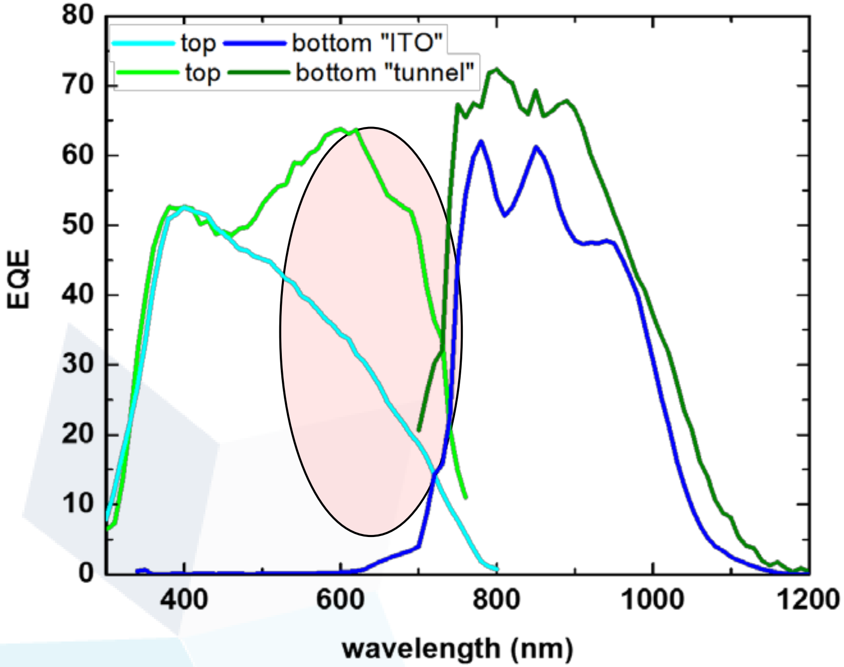




Interpretation:

- formation of a GaOx interface

Tandem cell with ITO degradation

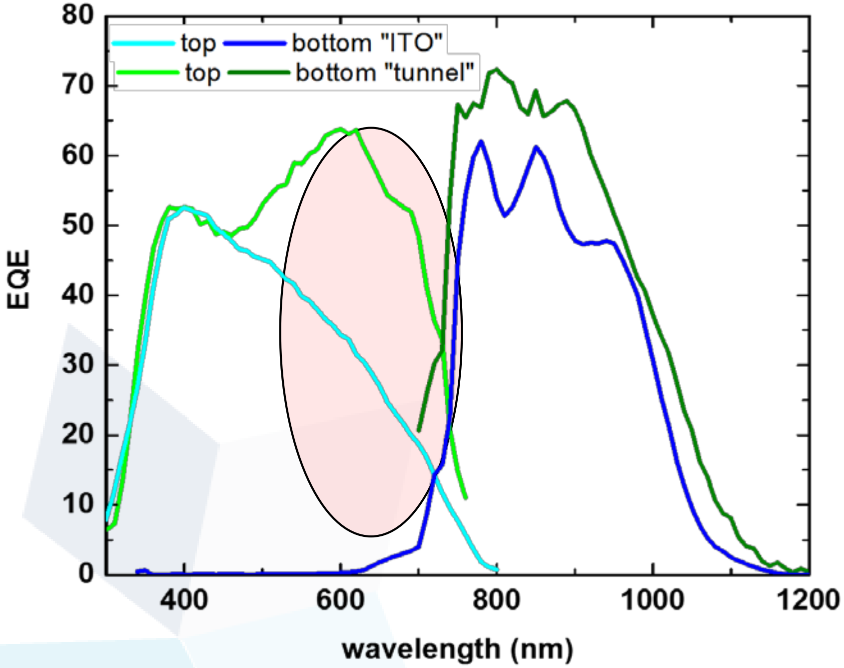


Tandem cell with ITO

CGSe back contact :

lower carrier collect

Tandem cell with ITO degradation



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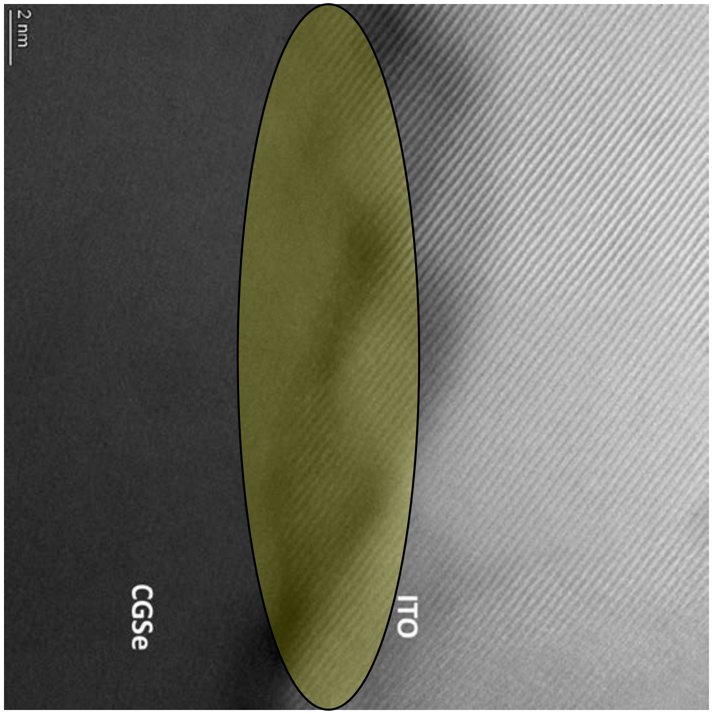


ITO / CGSe interface :
Formation of a GaOx interface

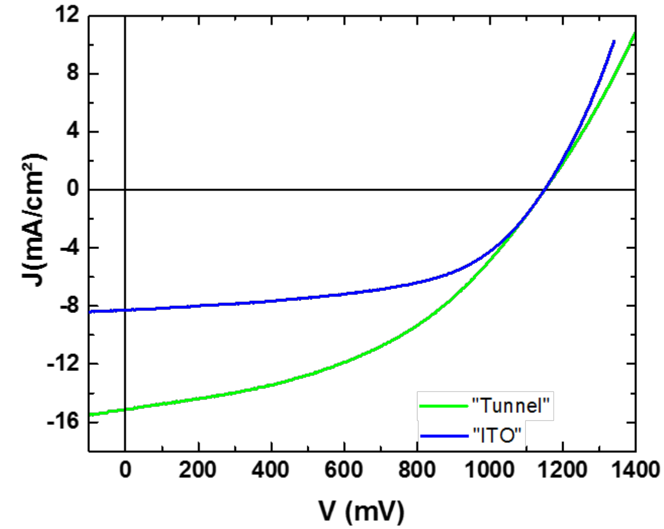
Conclusions & Perspectives

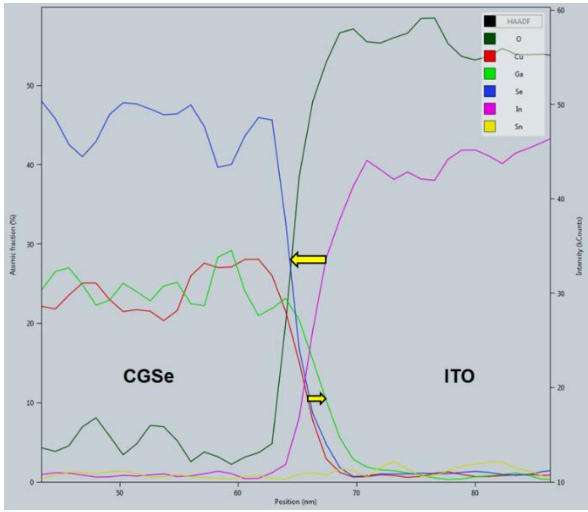
Tandem developments:

- Two fonctional tandem architectures had been made: **with ITO** and **with tunnel junction**

→ Tunnel: proof of concept and higher tandem efficiency

→ ITO: further development to avoid GaOx formation





Thank you for your attention

Tunnel junction analysis by ECV