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Industrialization of SHJ concepts

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HERCULES workshop – Konstanz 2015



Motivation - new PV generation

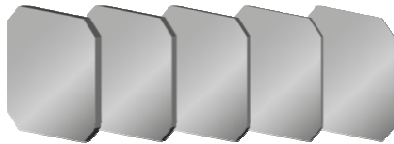


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A Diamond Wire

Thinner wafer → Lower costs

180 μm 160 μm 140 μm 120 μm 100 μm

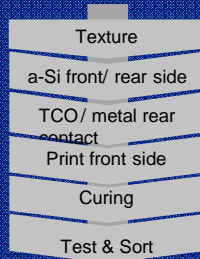


B Single Wafer Tracking

Quality & performance control



Heterojunction (HJT)



High efficiency

- Lower system cost (BOS)
- Independent of wafer thickness

Only 6 process steps

- Low COO

Temperature coefficient

- Higher energy yield
- Bifacial → Higher energy yield

C

D Adapted test metrology

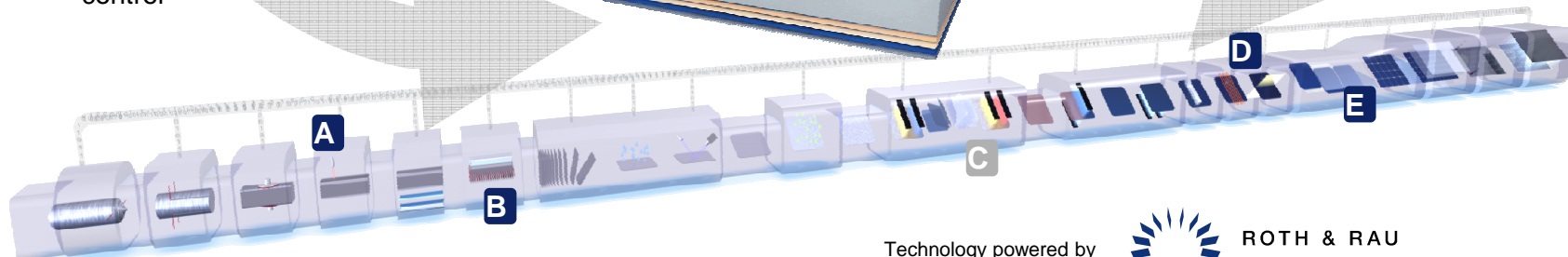
- High cap cells
- Busbarless cells
- DragonBack



E SmartWire Connection (SWCT)

TCO layer and wafer thickness suitable for SmartWire

- 80% less silver
- Higher energy yield
- Higher efficiency
- Longevity and micro-crack resistant



Outline



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- Heterojunction Cell Concept – Bifacial Rear Emitter
- Module Performance
- Status Demo Line
- First Cell Results in Ramp Up Phase



Outline



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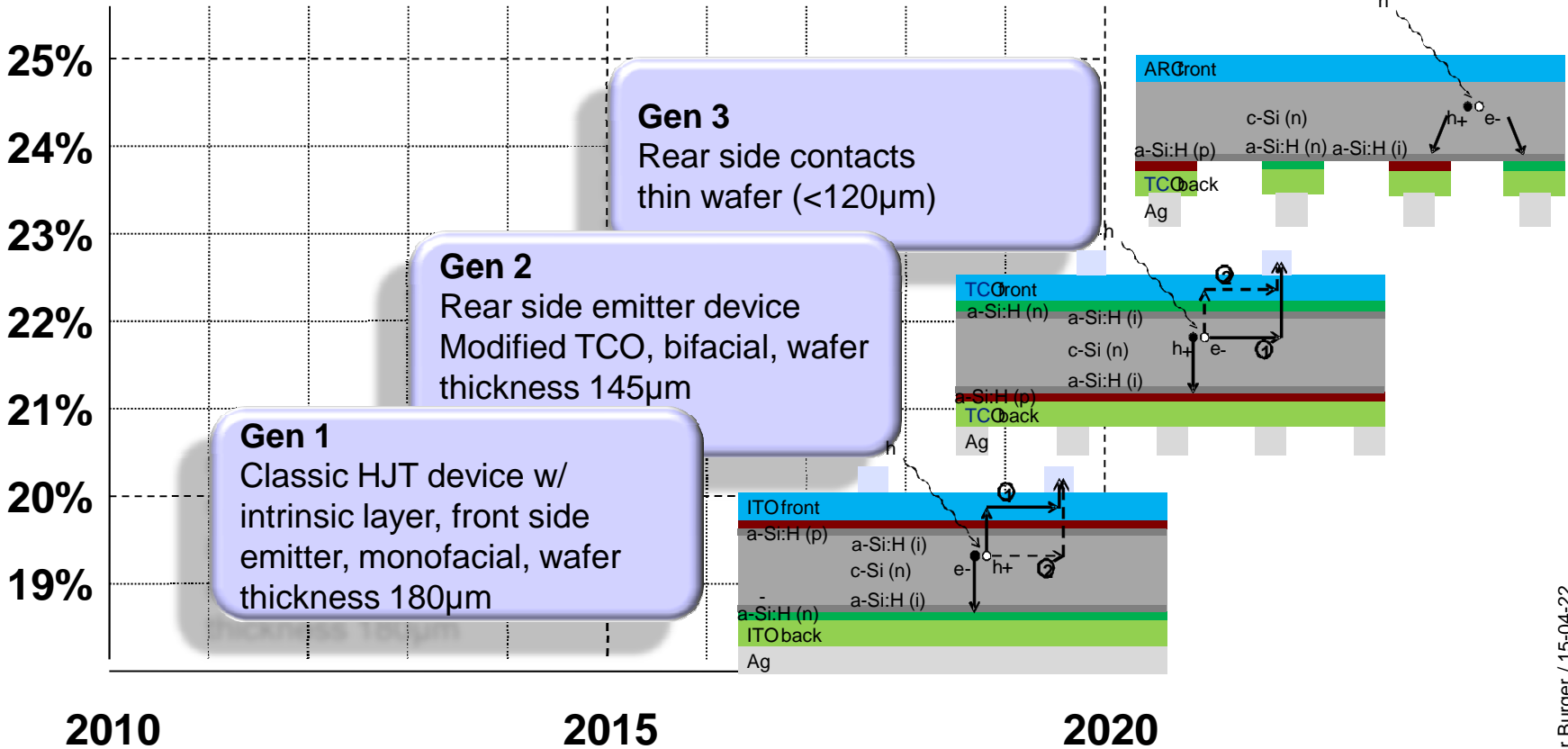
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Cell concepts/structures

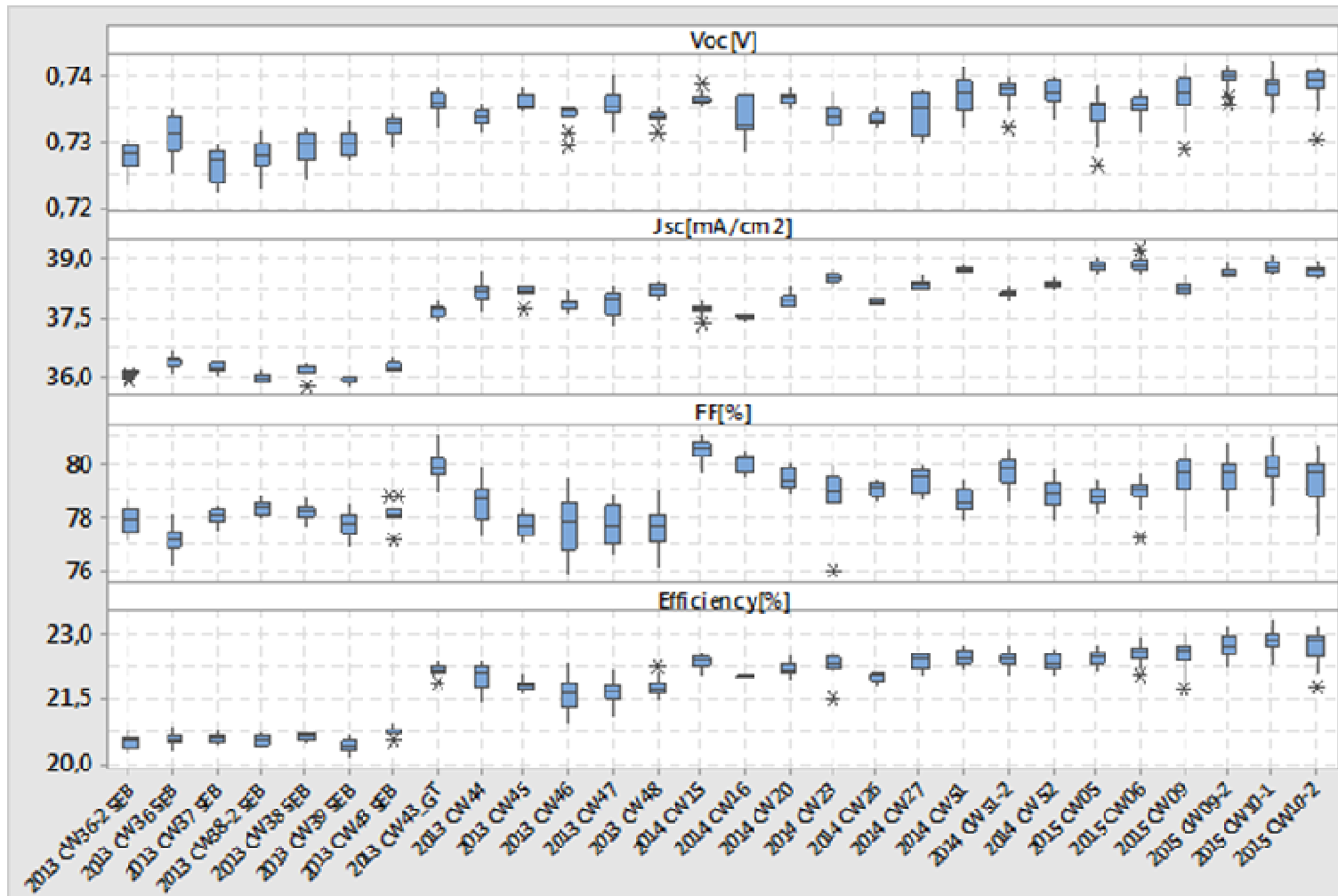
Long term technology roadmap



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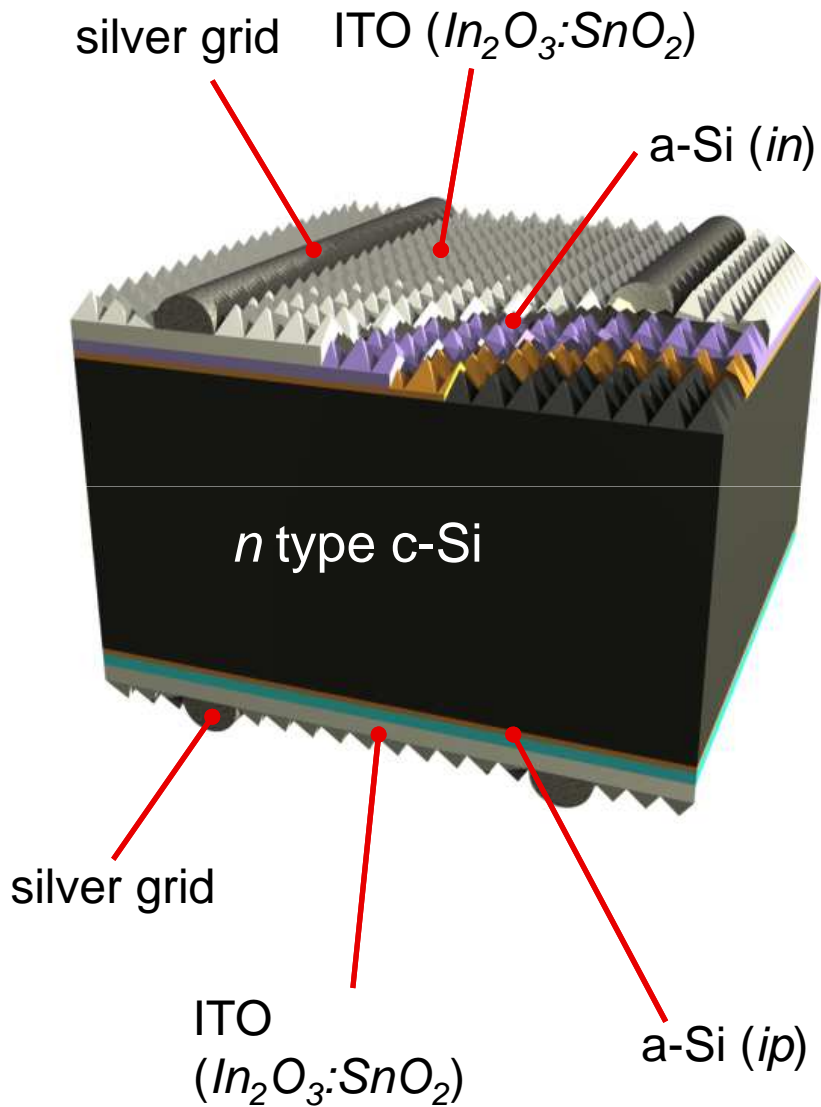


POR Monitoring SWCT

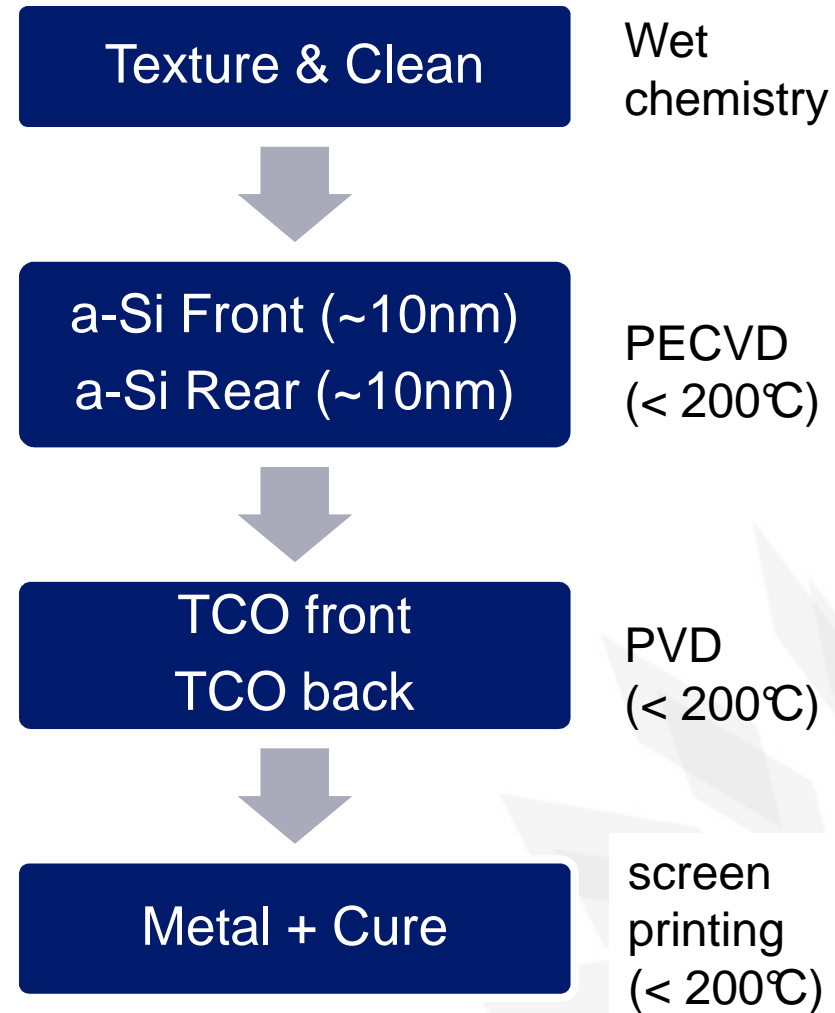


-> increase in I_{sc} , excellent FF

Si-HJT solar cell



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Outline



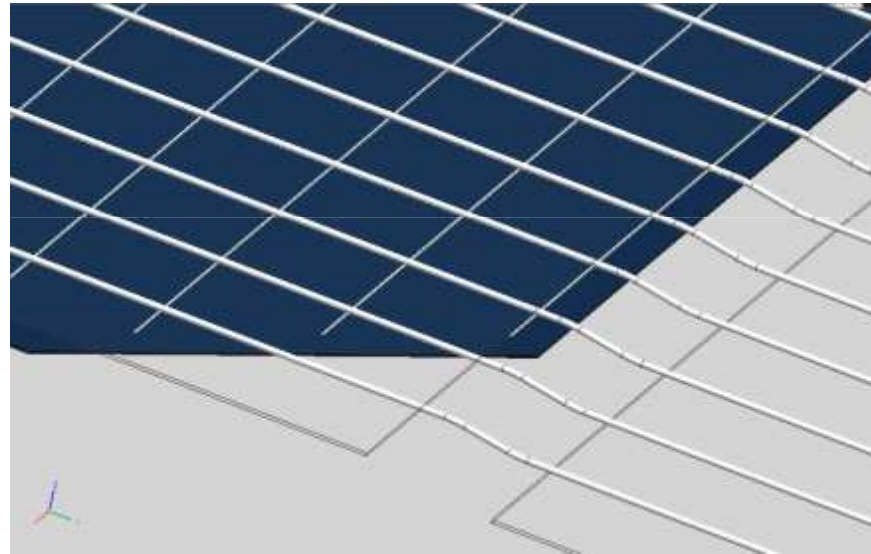
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- Heterojunction Cell Concept – Bifacial Rear Emitter
- **Module Performance**
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Concept combine bifacial SHJ cell with SWCT module



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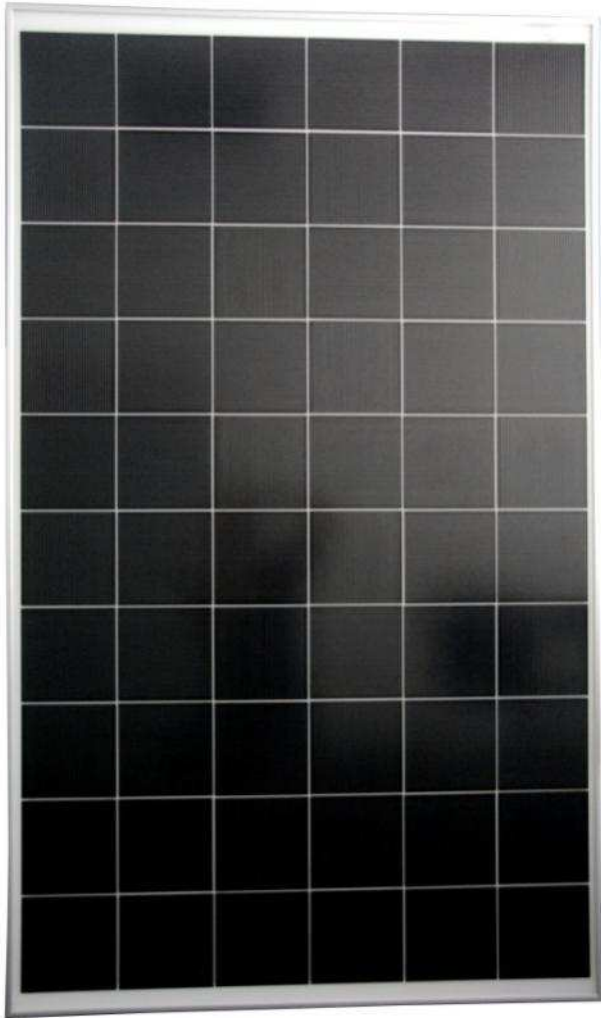


Concept & Performance

Best HJT + SWCT module power



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SUPSI



STS 531

P_{MPP}	327W
I_{sc}	9.5 A
V_{oc}	44.01 V
FF	78.2 %



Concept & Performance

HJT modules are quality tested



	<i>Initial</i>	<i>DH3000</i>	<i>DH4000</i>
Eff (%)	21.1	20.8	20.9
J _{SC} (mA/cm ²)	37.6	37.0	37.2
V _{OC} (mV/cell)	731	733	733
FF (%)	76.8	76.7	76.7
P _{max} (W)	308	304	305
Degradation	0.0	-1.3 %	-1.0 %

	<i>Initial</i>	<i>TC200</i>	<i>TC600</i>	<i>TC800</i>
P _{max} (W)	274	273	270	267
I _{SC} (A)	8.21	8.18	8.21	8.27
V _{OC} (V)	43.17	43.2	43.4	43.5
FF (%)	77.4	77.0	75.7	74.8
Degradation	0.0	-0.4%	-1.6%	-2.5%

Excellent Reliability
4 x IEC passed

[Faes, PVSEC 2014]



Concept & Performance

HJT SWCT module reliability proven



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**SGS
TÜV
SAAR**

IEC 61215
IEC 61730
Periodical Inspection



Certified by TÜV Saar according IEC 61215/61730, fire & PID testing included



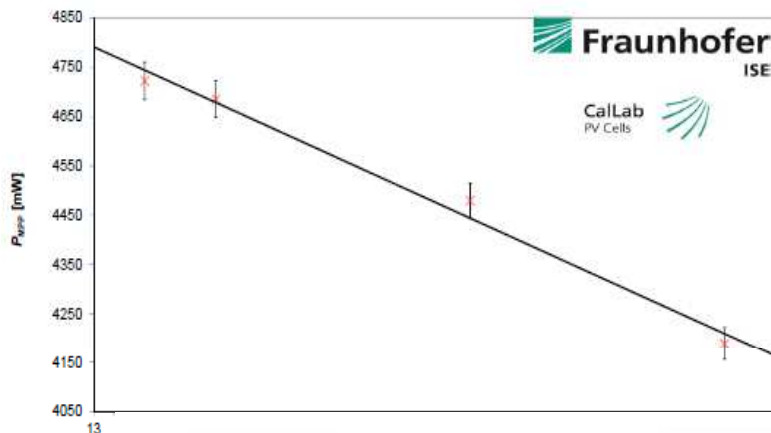
Concept & Performance

Superior temperature coefficient – high energy yield



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Power:
 $TK(P_{MPP}) = (-9.43 \pm 0.79) \text{ mW / K}$
 $TK(P_{MPP}) = (-0.201 \pm 0.017) \% / K$



-0,20 %/K on Cell level!

-0,22 %/K on Module level!

Test date [DD.MM.YYYY]		13.12.2012
Irradiance [W/m ²]		1000 ± 50
Module temperature [°C] high / low		56 / 22
Sample #	Coefficient	Calculated value
20120007554	α [% / K]	0.031
	β [% / K]	-0.200
	γ [% / K]	-0.219



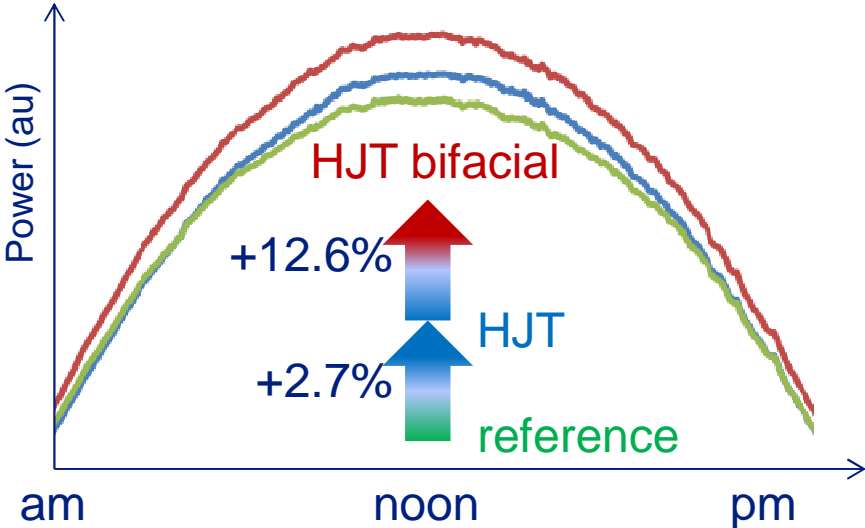
Excellent Temperature Coefficient certified by ISE CalLab and TÜV Rheinland!



Energy yield – reliability in the field



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+12.6% energy yield with HJT bifacial module compared to monofacial HJT.



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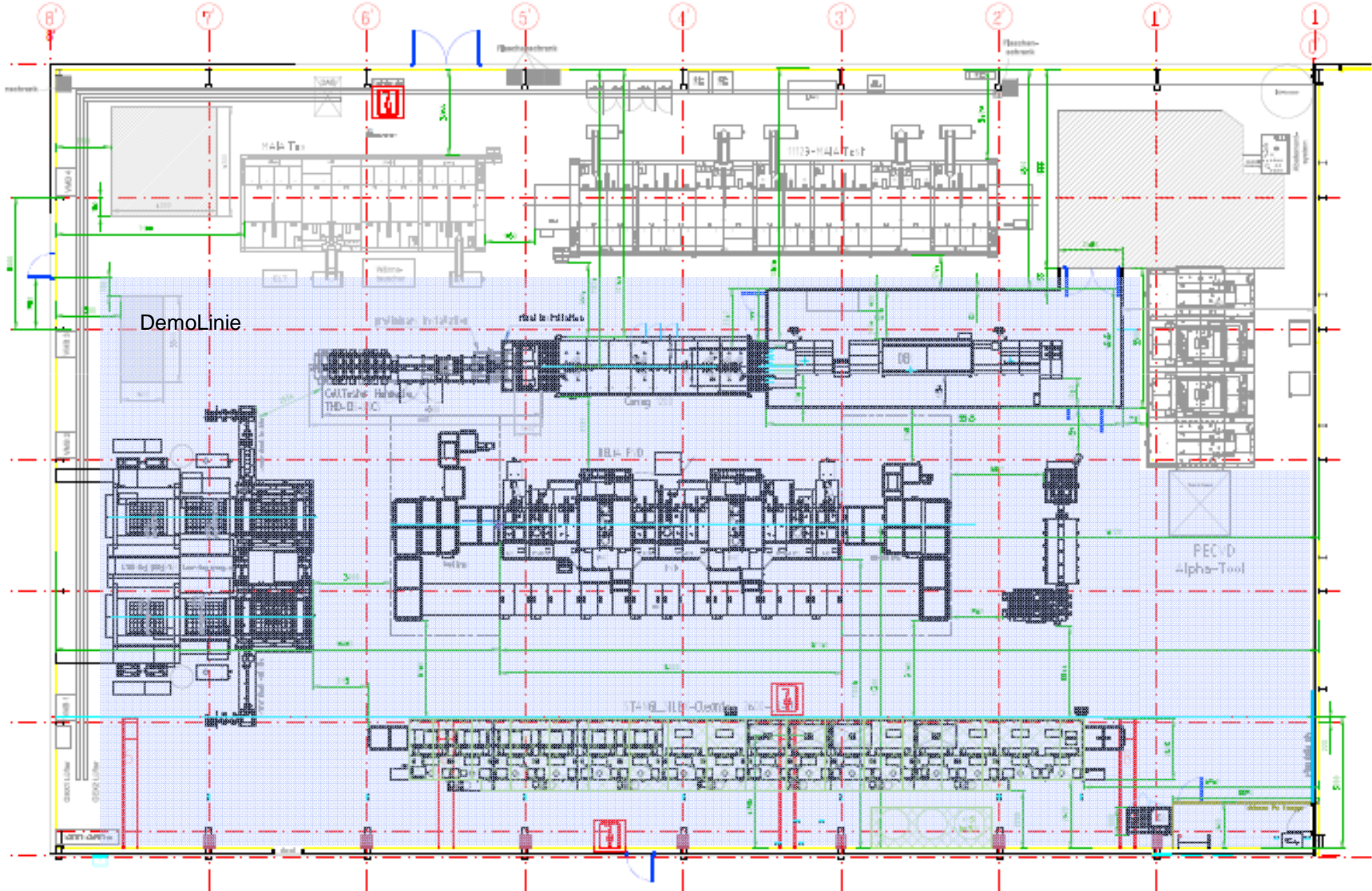
Demo cell line

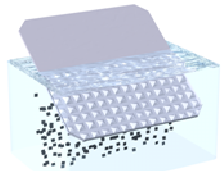


Demo cell line Layout



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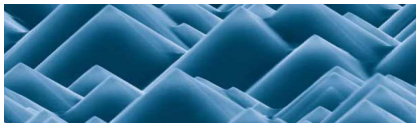
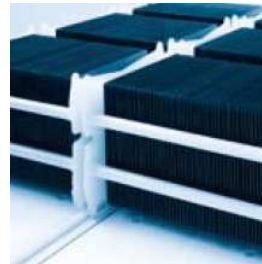




Processes Texturing and clean



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Wet Bench – Texturing & Clean

Advanced texturing & cleaning process for HJT solar cells

Alkaline Texturing and Cleaning

IPA free alkaline texturing

Automatic Carrier Handling System

- Process steps:
- Saw damage removal
 - Texturing
 - Clean and surface preparation

Texturing & clean

PECVD
a-Si:H

PVD
TCO + metal

Contact
Printing

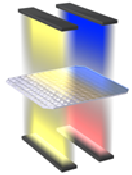
Curing

Test/Sort

Technology powered by



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CELL & COATING SYSTEMS



Processes PECVD a-Si:H



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HELiA_{PECVD} – Intrinsic and doped Si layer

PECVD system for the deposition of semiconductor and dielectric layers

Batch system with modular design and integrated automation

Excellent intrinsic and doped a-Si layer properties

Stable and uniform process without cross contamination

Low temperature processing: lowest production costs, compatible with thin wafers

Maintenance free chamber, dry clean

Texturing & clean

PECVD
a-Si:H

PVD
TCO + metal

Contact
Printing

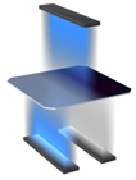
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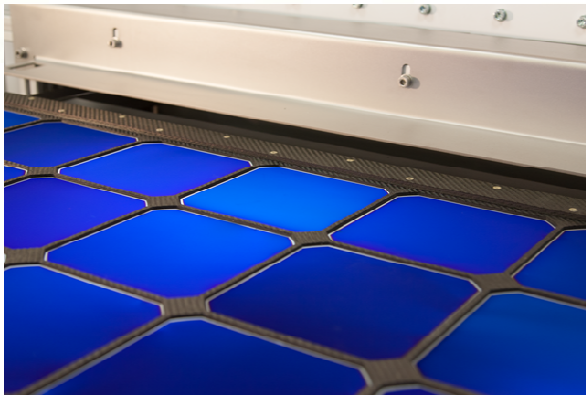
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Processes PVD TCO + metal



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HELiA_{PVD} – TCO and metal layer

PVD system for the deposition of TCO and metal layers

Double-side deposition in one pass through without wafer flipping

Integrated edge isolation

TCO and metal layers with excellent optical, electrical and mechanical performance

Inline system with integrated automation

Modular system: flexible coating-layer design, different custom stack-structures possible

Rotary magnetrons for high target utilization, long MTBM and short MTTM for low production cost

Texturing & clean

PECVD
a-Si:H

PVD
TCO + metal

Contact
Printing

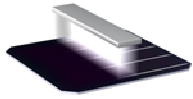
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Technology powered by



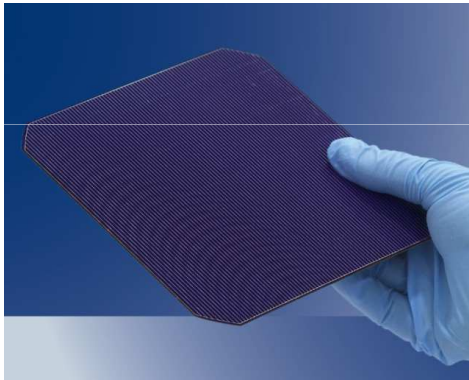
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Processes Fine line printing



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Metallization – Printing front contacts

High throughput metallization front side contacts

High speed screen printer with multiple and flexible printing modules

High accuracy and print repeatability

Integrated front side inspection and paste-saving automatic dispensing

Sensitive process adjustment

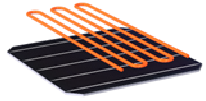
Low footprint



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Processes Curing



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CALiPSO – Flexible curing furnace

Using the flexible inline furnace platform CALiPSO in A-C-D configuration

Ceramic roller transport system for metal free and smooth cell transport

Precise temperature control and excellent temperature uniformity

Stable process conditions – excellent temperature uniformity ($\pm 2^\circ\text{C}$ across lanes)

Lower consumption due to thermal equilibrium and low heat loss

Texturing & clean

PECVD
a-Si:H

PVD
TCO + metal

Contact
Printing

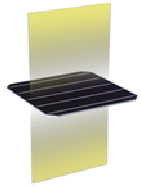
Curing

Test/Sort

Technology powered by



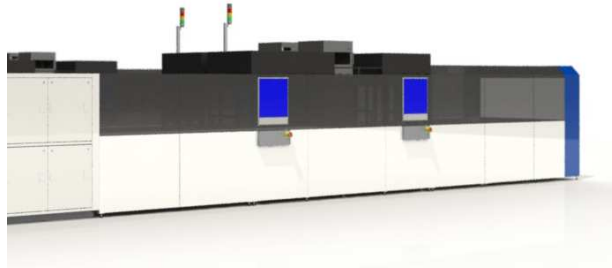
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Processes Test & Sort



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Tester & Sorter – SPOT^{LIGHT} technology

Cell testing & sorting system

Special flasher design for characterization of high capacitive HJT solar cells

Two parallel flasher for high throughput

EL integration optionally

Texturing & clean

PECVD
a-Si:H

PVD
TCO + metal

Contact
Printing

Curing

Test/Sort

Technology powered by



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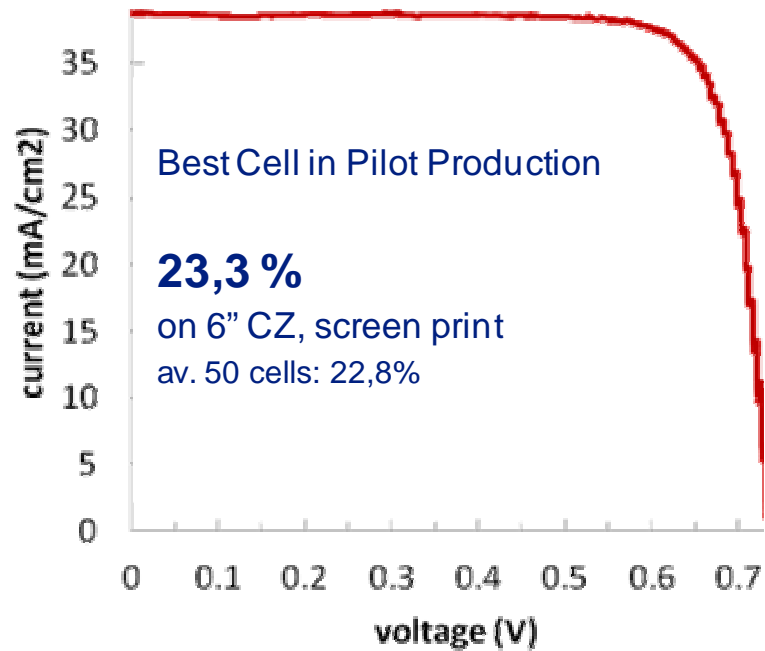


Concept & Performance

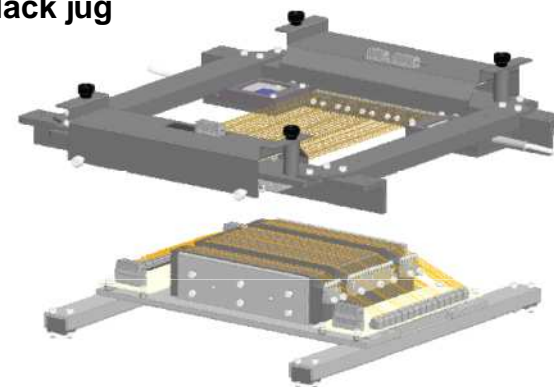
Champion cell on full production tool (BB-less)



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Grid^{TOUCH}
Contacting unit
black jug

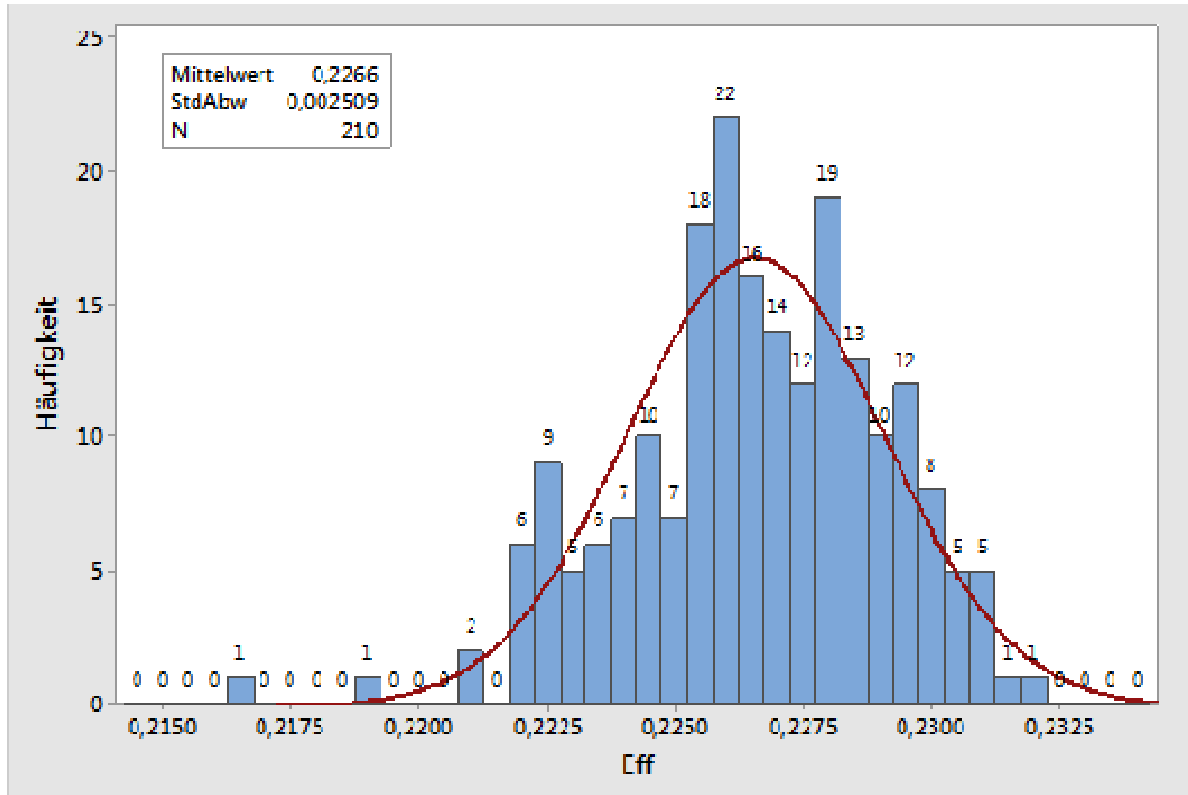


Status	Cell	Area (cm ²)	Eff. (%)	V _{oc} (mV)	FF (%)	J _{sc} (mA/cm ²)
March 2015	CZ	238.5	23.32	739	80,7	39,06
Dec 2013	FZ	238.5	23.5%	738.8	83.1	38.3



Rump UpTest

Cell efficiency distribution



Production run

March 2015

- Median 210 cells: 22,66% %
- Yield 98,1%



Next Steps



- further process window investigation
- Volume/Marathon testing, starting in May
- Manufacturing logistic optimization



Conclusion



- High Reliability for SHJ & SWCT certified
- Best Cell of Rear Emitter SHJ from production line >23% Eta
- av. 22,6% of 200 wafers in Ramp Up Phase

Thank you for your attention!



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